Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.4GHz)

| SPECrate®2017_int_base = | 282 |
| SPECrate®2017_int_peak = | Not Run |

<table>
<thead>
<tr>
<th>Copies</th>
<th>Test Date: Mar-2020</th>
<th>Hardware Availability: Feb-2020</th>
<th>Software Availability: May-2019</th>
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<td>520.ommnetpp_r 96</td>
<td>523.xalancbmk_r 96</td>
<td>525.x264_r 96</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6240R
- **Max MHz:** 4000
- **Nominal:** 2400
- **Enabled:** 48 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 35.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB SSD SATA
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None

**Power Management:** BIOS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

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<td>187</td>
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<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =  
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
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Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

**General Notes (Continued)**

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on linux-5vrl Sat Mar 14 11:22:25 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
  2 "physical id"s (chips)
   96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 24
  siblings : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 24 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):       32-bit, 64-bit
Byte Order:           Little Endian
CPU(s):               96
On-line CPU(s) list:  0-95
Thread(s) per core:   2
Core(s) per socket:   24
Socket(s):            2
NUMA node(s):         4
Vendor ID:            GenuineIntel
```

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_int_base = 282
SPECrater®2017_int_peak = Not Run

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,24-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92
NUMA node3 CPU(s): 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95

Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdempgb rtsc ep cmov

Warning: a numactl 'node' might or might not correspond to a physical chip.

From numactl --hardware

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrates®:
- SPECrates®2017_int_base = 282
- SPECrates®2017_int_peak = Not Run

Platform Notes (Continued)

node 3 free: 193036 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791164512 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 11:18

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 30G 193G 14% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSB-B200-M5
Serial: FCH22237D2V

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)                      |
|         | 525.x264_r(base) 557.xz_r(base)                                            |
==============================================================================

Intel® C Intel® 64 Compiler for applications running on Intel® 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)            |
|         | 541.leela_r(base)                                                          |
==============================================================================

Intel® C++ Intel® 64 Compiler for applications running on Intel® 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| Fortran | 548.exchange2_r(base)                                                      |
==============================================================================

Intel® Fortran Intel® 64 Compiler for applications running on Intel® 64,
Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

(Continued on next page)
Cisco Systems
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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/InteCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/InteCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/InteCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 6240R, 2.40GHz)

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**CPU2017 License:** 9019  
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The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-14 14:22:25-0400.  
Originally published on 2020-04-17.