**SPEC CPU®2017 Integer Rate Result**

**Fujitsu**

PRIMERGY RX2540 M5, Intel Xeon Silver 4214R, 2.40 GHz

**SPECrate®2017_int_base = 133**

**SPECrate®2017_int_peak = 139**

---

**Hardware**

- **CPU Name:** Intel Xeon Silver 4214R
- **Max MHz:** 3500
- **Nominal:** 2400
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Other:** None

**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)

**Storage:** 1 x SATA M.2 SSD, 240 GB

**Other:** None

---

**Software**

- **OS:** SUSE Linux Enterprise Server 15
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
- **Parallel:** No
- **Firmware:** Fujitsu BIOS Version V5.0.0.14 R1.18.0 for D3384-B1x released Apr-2020
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc: jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

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**CPU2017 License:** 19

**Test Sponsor:** Fujitsu

**Test Date:** Mar-2020

**Hardware Availability:** May-2019

**Tested by:** Fujitsu

**Software Availability:** May-2019

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**Copies**

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Fujitsu
PRIMERGY RX2540 M5, Intel Xeon Silver 4214R, 2.40 GHz

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Fujitsu

SPECrate®2017_int_base = 133
SPECrate®2017_int_peak = 139

Results Table

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<td>601</td>
<td>86.3</td>
<td>601</td>
<td>86.2</td>
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</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"
Kernel Boot Parameter set with: nohz_full=1-47

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/Benchmark/cpu2017-1.1.0/lib/intel64:/home/Benchmark/cpu2017-1.1.0/lib/ia32:/home/Benchmark/cpu2017-1.1.0/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets

(Continued on next page)
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**CPU2017 License:** 19  
**Test Sponsor:** Fujitsu  
**Tested by:** Fujitsu  
**Test Date:** Mar-2020  
**Hardware Availability:** May-2019  
**Software Availability:** May-2019

---

**General Notes (Continued)**

jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5  
jemalloc: sources available via jemalloc.net  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)  
is mitigated in the system as tested and documented.

---

**Platform Notes**

BIOS configuration:  
Stale AtoS = Enabled  
Patrol Scrub = Disabled  
WR CRC feature Control = Disabled  
Fan Control = Full

Sysinfo program /home/Benchmark/cpu2017-1.1.0/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edbi6e6e46a485a0011  
running on sles15 Wed Mar 11 08:22:34 2020

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz  
2 "physical id"s (chips)  
48 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 12  
siblings : 24  
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13  
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:  
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 48  
On-line CPU(s) list: 0-47  
Thread(s) per core: 2  
Core(s) per socket: 12

(Continued on next page)
Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-2, 6-8, 24-26, 30-32
NUMA node1 CPU(s): 3-5, 9-11, 27-29, 33-35
NUMA node2 CPU(s): 12-14, 18-20, 36-38, 42-44
NUMA node3 CPU(s): 15-17, 21-23, 39-41, 45-47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xptr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm ablahf_1m ablahf_1m ablahf_1m ablahf_1m ablahf_1m ablahf_1m

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

(Continued on next page)
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Platform Notes (Continued)

node 2 free: 193279 MB
node 3 cpus: 15 16 17 21 22 23 39 40 41 45 46 47
node 3 size: 193532 MB
node 3 free: 193297 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791163176 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

uname -a:
Linux sles15 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 11 08:16

SPEC is set to: /home/Benchmark/cpu2017-1.1.0

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 ext4 188G 33G 146G 19% /

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Software Availability: May-2019

Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: FUJITSU // American Megatrends Inc. V5.0.0.14 R1.18.0 for D3384-B1x
02/10/2020
Vendor: FUJITSU
Product: PRIMERGY RX2540 M5
Product Family: SERVER
Serial: YMSQXXXXXX

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
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## Compiler Version Notes (Continued)

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<td>C++</td>
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CPU2017 License: 19
Test Sponsor: Fujitsu
Tested by: Fujitsu
Test Date: Mar-2020
Hardware Availability: May-2019
Software Availability: May-2019

Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

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Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Compiler Invocation

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

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---

**Peak Optimization Flags (Continued)**

500.perlbench_r (continued):
- fno-strict-overflow
- L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

502.gcc_r: -Wl, -z, muldefs -prof-gen (pass 1) -prof-use (pass 2) -ipo
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -fno-alias
- L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

557.xz_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: -Wl, -z, muldefs -prof-gen (pass 1) -prof-use (pass 2) -ipo
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

---

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


http://www.spec.org/cpu2017/flags/Fujitsu-Platform-Settings-V1.0-CSL-RevE.xml
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</tr>
</tbody>
</table>

- Test Date: Mar-2020  
- Hardware Availability: May-2019  
- Software Availability: May-2019

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