Hewlett Packard Enterprise  
Synergy 480 Gen10  
(3.20 GHz, Intel Xeon Silver 4215R)  

| Threads | 0 | 15.0 | 30.0 | 45.0 | 60.0 | 75.0 | 90.0 | 105 | 120 | 135 | 150 | 165 | 180 | 195 | 210 | 225 | 240 | 255 | 270 | 285 | 300 |
|---------|---|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 603.bwaves_s 16 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 | 85.3 | 83.4 |
| 607.cactuBSSN_s 16 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 | 67.7 |
| 619.lbm_s 16 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 | 81.7 |
| 621.wrf_s 16 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 | 41.2 | 41.3 |
| 627.cam4_s 16 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 | 51.9 |
| 628.pop2_s 16 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 | 61.1 |
| 638.imagick_s 16 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 | 61.0 |
| 644.nab_s 16 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 | 117 |
| 654.roms_s 16 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 | 70.6 |

--- SPECspeed®2017_fp_base (78.8) ---  
--- SPECspeed®2017_fp_peak (79.4) ---

**Hardware**

- **CPU Name:** Intel Xeon Silver 4215R  
- **Max MHz:** 4000  
- **Nominal:** 3200  
- **Enabled:** 16 cores, 2 chips  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
- **Kernel:** 4.12.14-195-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;  
- **Parallel:** Yes  
- **Firmware:** HPE BIOS Version I42 v2.22 (11/13/2019) released Apr-2020  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Base</th>
<th>Peak</th>
<th>Peak</th>
<th>Ratio</th>
<th>Base</th>
<th>Base</th>
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<th>Peak</th>
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<tr>
<td>603.bwaves_s</td>
<td>16</td>
<td>196 302</td>
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<tr>
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<td>16</td>
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<td>77.4 67.7</td>
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<td>162 81.7</td>
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<tr>
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<td>227 52.3</td>
<td>229 51.9</td>
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<tr>
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</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base = 78.8**  
**SPECspeed®2017_fp_peak = 79.4**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

- Stack size set to unlimited using "ulimit -s unlimited"
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  - `sync; echo 3> /proc/sys/vm/drop_caches`

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- `KMP_AFFINITY = "granularity=fine,compact"`
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"`
- `OMP_STACKSIZE = "192M"`

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU®2017 Floating Point Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

SPECspeed®2017_fp_base = 78.8
SPECspeed®2017_fp_peak = 79.4

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Intel UPI Link Power Management set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbb1e6e46a485a0011
running on sy480-sys1 Mon Mar 16 23:41:30 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
   2 "physical id"s (chips)
   16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz

(Continued on next page)
Hewlett Packard Enterprise
Synergy 480 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

<table>
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<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Jun-2019</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

Stepping:              7
CPU MHz:               3200.000
BogoMIPS:              6400.00
Virtualization:       VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              11264K
NUMA node0 CPU(s):    0-7
NUMA node1 CPU(s):    8-15
Flags:                fpu vme de pse tsc msr pae mce cmov
                      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                      lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                      aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
                      xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                      avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
                      invpcid_single intel_pni ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi
                      flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm
                      cqm mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
                      avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsave cqm_llc cqm_occcll cc qm_mbm_total
                      cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld
                      arch_capabilities

/proc/cpuinfo cache data
    cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7
    node 0 size: 193057 MB
    node 0 free: 192749 MB
    node 1 cpus: 8 9 10 11 12 13 14 15
    node 1 size: 193308 MB
    node 1 free: 192875 MB
    node distances:
        node 0 1
        0: 10 21
        1: 21 10

From /proc/meminfo
    MemTotal: 395638896 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
    os-release:
SPEC CPU®2017 Floating Point Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

SPECspeed®2017_fp_base = 78.8
SPECspeed®2017_fp_peak = 79.4

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux sy480-sys1 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 16 23:39

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 371G 97G 274G 27% /home

From /sys/devices/virtual/dmi/id
BIOS: HPE I42 11/13/2019
Vendor: HPE
Product: Synergy 480 Gen10
Product Family: Synergy
Serial: MXQ7380505

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

SPECspeed®2017_fp_base = 78.8
SPECspeed®2017_fp_peak = 79.4

Compiler Version Notes

==============================================================================
C
| 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran
| 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C
| 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
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SPECspeed®2017_fp_base = 78.8
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Peak Optimization Flags (Continued)

654.roms_s (continued):
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-DSPEC_OPENMP -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-16 23:41:30-0400.