### SPEC CPU®2017 Integer Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.40 GHz, Intel Xeon Silver 4210R)

**SPECrate®2017_int_base = 114**  
**SPECrate®2017_int_peak = 119**

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (114)</th>
<th>SPECrate®2017_int_peak (119)</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>83.9</td>
<td>96.3</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>93.6</td>
<td>107</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>77.2</td>
<td>133</td>
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<tr>
<td>520.omnetpp_r</td>
<td>76.4</td>
<td>132</td>
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<tr>
<td>523.xalancbmk_r</td>
<td>74.0</td>
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<td>525.x264_r</td>
<td>83.9</td>
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<td>531.deepsjeng_r</td>
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<td>88.1</td>
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<td>548.exchange2_r</td>
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</tr>
<tr>
<td>557.xz_r</td>
<td>74.0</td>
<td>242</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4210R  
- **Max MHz:** 3200  
- **Nominal:** 2400  
- **Enabled:** 20 cores, 2 chips, 2 threads/core  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
- **Kernel:** 4.12.14-195-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;  
- **Parallel:** No  
- **Firmware:** HPE BIOS Version I42 v2.22 (11/13/2019) released Apr-2020  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>583</td>
<td>74.1</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
Hewlett Packard Enterprise  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.40 GHz, Intel Xeon Silver 4210R)  

SPECrate®2017_int_base = 114  
SPECrate®2017_int_peak = 119

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>3</th>
<th>Test Date:</th>
<th>Mar-2020</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>HPE</td>
<td>Hardware Availability:</td>
<td>Apr-2020</td>
</tr>
<tr>
<td>Tested by:</td>
<td>HPE</td>
<td>Software Availability:</td>
<td>Jun-2019</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


**Platform Notes**

BIOS Configuration:  
Thermal Configuration set to Maximum Cooling  
Memory Patrol Scrubbing set to Disabled  
LLC Prefetch set to Enabled  
LLC Dead Line Allocation set to Disabled  
Enhanced Processor Performance set to Enabled  
Workload Profile set to General Throughput Compute  
Workload Profile set to Custom  
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f88a3d7edb1e6e46a485a0011  
running on sy480-sys2 Fri Mar 13 07:44:20 2020

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz  
  2 "physical id"s (chips)  
  40 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
  cpu cores : 10  
  siblings : 20  
  physical 0: cores 0 1 2 3 4 8 9 10 11 12  
  physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:  
  Architecture:        x86_64  
  CPU op-mode(s):      32-bit, 64-bit  
  Byte Order:          Little Endian  
  Address sizes:       46 bits physical, 48 bits virtual

(Continued on next page)
Hewlett Packard Enterprise
Synergy 480 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

SPEC CPU®2017 Integer Rate Result

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Test Sponsor: HPE
Hardware Availability: Apr-2020
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CPU2017 License: 3
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Tested by: HPE

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CPU(s): 40
On-line CPU(s) list: 0–39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0–9, 20–29
NUMA node1 CPU(s): 10–19, 30–39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpf1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrig pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pni ssbd mba ibrs ibpb ibrs enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rspeed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld
arch_capabilities

/platform/cpuinfo/cache_data
cache size: 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0–1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 193054 MB
node 0 free: 192643 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 193304 MB
node 1 free: 192885 MB
node distances:
node 0 1

(Continued on next page)
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Platform Notes (Continued)

0:  10  21
1:  21  10

From /proc/meminfo
MemTotal:       395632264 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
  Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 13 07:42

SPEC is set to: /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sda2      btrfs  371G  116G  255G  32% /home

From /sys/devices/virtual/dmi/id
BIOS:        HPE I42 11/13/2019
Vendor:      HPE
Product:     Synergy 480 Gen10
Product Family: Synergy
Serial:      MXQ72204FC

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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C | 502.gcc_r(peak)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
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Software Availability: Jun-2019

Compiler Version Notes (Continued)

C++ | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

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**Base Compiler Invocation (Continued)**

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

**Base Portability Flags**

- **C benchmarks:**
  -500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
  -502.gcc_r: -DSPEC_LP64
  -505.mcf_r: -DSPEC_LP64
  -520.omnetpp_r: -DSPEC_LP64
  -523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
  -525.x264_r: -DSPEC_LP64
  -531.deepsjeng_r: -DSPEC_LP64
  -541.leela_r: -DSPEC_LP64
  -548.exchange2_r: -DSPEC_LP64
  -557.xz_r: -DSPEC_LP64

- **C++ benchmarks:**
  -500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
  -502.gcc_r: -DSPEC_LP64
  -505.mcf_r: -DSPEC_LP64
  -520.omnetpp_r: -DSPEC_LP64
  -523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
  -525.x264_r: -DSPEC_LP64
  -531.deepsjeng_r: -DSPEC_LP64
  -541.leela_r: -DSPEC_LP64
  -548.exchange2_r: -DSPEC_LP64
  -557.xz_r: -DSPEC_LP64

**Base Optimization Flags**

- **C benchmarks:**
  -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

- **C++ benchmarks:**
  -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

- **Fortran benchmarks:**
  -Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc
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CPU2017 License: 3  
Test Sponsor: HPE  
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Test Date: Mar-2020  
Hardware Availability: Apr-2020  
Software Availability: Jun-2019  

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc -m64 -std=c11

C++ benchmarks (except as noted below):
  icpc -m64
  523.xalancbmk_r:icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
  ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -D_FILE_OFFSET_BITS=64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
  500.perlbench_r: -Wl,-z,xmuldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
  -fno-strict-overflow  
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
  -lqkmalloc
  502.gcc_r: -Wl,-z,xmuldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
  -L/usr/local/jee5.0.1-32/lib -ljemalloc
  505.mcf_r: -Wl,-z,xmuldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=4

(Continued on next page)
### Peak Optimization Flags (Continued)

505.mcf_r (continued):
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

525.x264_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -fno-alias`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

523.xalancbmk_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo`
- `-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4`
- `-L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

| SPECrate®2017_int_base = 114 |
| SPECrate®2017_int_peak = 119 |

| CPU2017 License: 3 | Test Date: Mar-2020 |
| Test Sponsor: HPE | Hardware Availability: Apr-2020 |
| Tested by: HPE | Software Availability: Jun-2019 |

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Tested with SPEC CPU®2017 v1.1.0 on 2020-03-13 07:44:20-0400.