SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(1.90 GHz, Intel Xeon Bronze 3206R)

SPECrat®2017_int_base = 53.1
SPECrat®2017_int_peak = 54.0

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Hardware
CPU Name: Intel Xeon Bronze 3206R
Max MHz: 1900
Nominal: 1900
Enabled: 16 cores, 2 chips
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)
Storage: 1 x 400 GB SAS SSD, RAID 0
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)
Kernel 4.12.14-195-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;
Parallel: No
Firmware: HPE BIOS Version I42 v2.22 (11/13/2019) released Apr-2020
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>16</td>
<td>607</td>
<td>42.0</td>
<td>606</td>
<td>42.0</td>
<td>609</td>
<td>41.9</td>
<td>16</td>
<td>538</td>
<td>47.4</td>
<td>538</td>
<td>47.4</td>
<td>539</td>
<td>47.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>16</td>
<td>452</td>
<td>50.2</td>
<td>451</td>
<td>50.2</td>
<td>452</td>
<td>50.1</td>
<td>16</td>
<td>425</td>
<td>53.3</td>
<td>426</td>
<td>53.2</td>
<td>426</td>
<td>53.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>16</td>
<td>415</td>
<td>62.4</td>
<td>414</td>
<td>62.4</td>
<td>414</td>
<td>62.4</td>
<td>16</td>
<td>413</td>
<td>62.6</td>
<td>414</td>
<td>62.4</td>
<td>414</td>
<td>62.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>16</td>
<td>528</td>
<td>39.7</td>
<td>531</td>
<td>39.6</td>
<td>529</td>
<td>39.7</td>
<td>16</td>
<td>532</td>
<td>39.5</td>
<td>531</td>
<td>39.5</td>
<td>528</td>
<td>39.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>16</td>
<td>260</td>
<td>65.0</td>
<td>261</td>
<td>64.8</td>
<td>260</td>
<td>64.9</td>
<td>16</td>
<td>270</td>
<td>62.5</td>
<td>269</td>
<td>62.8</td>
<td>270</td>
<td>62.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>16</td>
<td>258</td>
<td>109</td>
<td>258</td>
<td>109</td>
<td>258</td>
<td>109</td>
<td>16</td>
<td>247</td>
<td>113</td>
<td>247</td>
<td>113</td>
<td>247</td>
<td>113</td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>16</td>
<td>431</td>
<td>42.5</td>
<td>431</td>
<td>42.5</td>
<td>431</td>
<td>42.5</td>
<td>16</td>
<td>432</td>
<td>42.5</td>
<td>431</td>
<td>42.5</td>
<td>431</td>
<td>42.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>16</td>
<td>768</td>
<td>34.5</td>
<td>768</td>
<td>34.5</td>
<td>768</td>
<td>34.5</td>
<td>16</td>
<td>769</td>
<td>34.4</td>
<td>770</td>
<td>34.4</td>
<td>770</td>
<td>34.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>16</td>
<td>568</td>
<td>30.4</td>
<td>568</td>
<td>30.4</td>
<td>569</td>
<td>30.4</td>
<td>16</td>
<td>568</td>
<td>30.4</td>
<td>569</td>
<td>30.4</td>
<td>568</td>
<td>30.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesyste page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
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Synergy 480 Gen10
(1.90 GHz, Intel Xeon Bronze 3206R)

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SPECrate®2017_int_peak = 54.0

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edeb1e6e46a485a0011
running on sy480-sys2 Tue Mar 24 10:55:50 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
 2 "physical id"s (chips)
 16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual

(Continued on next page)
### Platform Notes (Continued)

```plaintext
CPU(s):              16
On-line CPU(s) list: 0-15
Thread(s) per core:  1
Core(s) per socket:  8
Socket:              2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping:            7
CPU MHz:             1900.000
BogoMIPS:            3800.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            11264K
NUMA node0 CPU(s):   0-3,8-11
NUMA node1 CPU(s):   4-7,12-15
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                      lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                      aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
                      xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                      avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
                      invpcid_single intel_pppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
                      flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ervs invpcid rtm
                      cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
                      avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
                      cqm_mbb_local dtherm arat pln pts pku ospke avx512_vnni md_clear flush_l1d
                      arch_capabilities
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
```
available:  2 nodes (0-1)
node 0 cpus:  0 1 2 3 8 9 10 11
node 0 size:  193057 MB
node 0 free:  192594 MB
node 1 cpus:  4 5 6 7 12 13 14 15
node 1 size:  193307 MB
node 1 free:  193020 MB
node distances:
node   0  1
```

(Continued on next page)
Hewlett Packard Enterprise
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 395637872 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 24 10:53

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
BIOS: HPE I42 11/13/2019
Vendor: HPE
Product: Synergy 480 Gen10
Product Family: Synergy
Serial: MXQ72204FC

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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<table>
<thead>
<tr>
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<th>Test Date: Mar-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Apr-2020</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Jun-2019</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 53.1

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Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
       | 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(1.90 GHz, Intel Xeon Bronze 3206R)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

HPE

Compiler Version Notes (Continued)

C++ | 523.xalancbmk_r(peak)

|-- Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

|-- C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
|   | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

|-- Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

|-- C++ | 523.xalancbmk_r(peak)

|-- Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

|-- C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
|   | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

|-- Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

|-- Fortran | 548.exchange2_r(base, peak)

|-- Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

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# SPEC CPU®2017 Integer Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
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<table>
<thead>
<tr>
<th>Spec CPU®2017 Integer Rate Result</th>
<th>Test Sponsor: HPE</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>SPECrate®2017_int_base</strong> = 53.1</td>
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<td><strong>Software Availability</strong>: Jun-2019</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Tested by: HPE</th>
</tr>
</thead>
</table>

## Base Compiler Invocation (Continued)

C++ benchmarks:
```
icpc -m64```

Fortran benchmarks:
```
ifort -m64```

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>gcc_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

### C benchmarks:
```
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc```

### C++ benchmarks:
```
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc```

### Fortran benchmarks:
```
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/Intel Compiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc```

---

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Standard Performance Evaluation Corporation (info@spec.org)  
https://www.spec.org/
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</tr>
</thead>
<tbody>
<tr>
<td>Tested by</td>
<td>HPE</td>
<td>Test Date</td>
<td>Mar-2020</td>
</tr>
<tr>
<td>CPU2017 License</td>
<td>3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Peak Compiler Invocation**

C benchmarks (except as noted below):
```bash
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

**Peak Portability Flags**

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`
- `531.deepsjeng_r: -DSPEC_LP64`
- `541.leela_r: -DSPEC_LP64`
- `548.exchange2_r: -DSPEC_LP64`
- `557.xz_r: -DSPEC_LP64`

**Peak Optimization Flags**

C benchmarks:
```bash
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc
```

```bash
502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```bash
505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
```

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r -W1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml
<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hewlett Packard Enterprise</strong></td>
</tr>
<tr>
<td>(Test Sponsor: HPE)</td>
</tr>
<tr>
<td><strong>Synergy 480 Gen10</strong></td>
</tr>
<tr>
<td>(1.90 GHz, Intel Xeon Bronze 3206R)</td>
</tr>
<tr>
<td><strong>SPECrater®2017_int_base = 53.1</strong></td>
</tr>
<tr>
<td><strong>SPECrater®2017_int_peak = 54.0</strong></td>
</tr>
</tbody>
</table>

| CPU2017 License: | 3 |
| Test Sponsor: | HPE |
| Tested by: | HPE |
| Test Date: | Mar-2020 |
| Hardware Availability: | Apr-2020 |
| Software Availability: | Jun-2019 |

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-24 10:55:49-0400.  