## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

<table>
<thead>
<tr>
<th>Test Sponsor</th>
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### SPECspeed®2017_fp_base = 150

### SPECspeed®2017_fp_peak = Not Run

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (150)</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>40</td>
<td>151</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>40</td>
<td>169</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>40</td>
<td>107</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>40</td>
<td>139</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>40</td>
<td>111</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>40</td>
<td>67.6</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>40</td>
<td>148</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>40</td>
<td>26</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>40</td>
<td>87.7</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>40</td>
<td>151</td>
</tr>
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### Hardware

- **CPU Name:** Intel Xeon Gold 6242R
- **Max MHz:** 4100
- **Nominal:** 3100
- **Enabled:** 40 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 35.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB SSD SAS
- **Other:** None
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None

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**Standard Performance Evaluation Corporation (info@spec.org) [https://www.spec.org/](https://www.spec.org/)**
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SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 150
SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
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<tr>
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<td>111</td>
<td>531</td>
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<td>544</td>
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<td>546</td>
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<td>607.cactuBSSN_s</td>
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<td>98.8</td>
<td>169</td>
<td>99.0</td>
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<td>152</td>
<td>104</td>
<td>151</td>
</tr>
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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)  

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SPECspeed®2017_fp_base = 150
SPECspeed®2017_fp_peak = Not Run

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1b6e46a485a0011
running on linux-5vrl Mon Apr 13 07:31:58 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
2 "physical id"s (chips)
40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 5 6 10 11 12 13 16 17 18 19 21 24 26 27 28 29
physical 1: cores 0 1 2 3 5 6 9 10 12 13 16 17 18 19 20 21 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
Stepping: 7
CPU MHz: 3100.000
CPU max MHz: 4100.0000
CPU min MHz: 1200.0000
BogoMIPS: 6200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
Cisco Systems
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SPECspeed®2017_fp_base = 150
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Platform Notes (Continued)

L2 cache:            1024K
L3 cache:            36088K
NUMA node0 CPU(s):   0-19
NUMA node1 CPU(s):   20-39

Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref perf_event_pagesize tsc_actual_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat _13 cpd _13 invpcid_single intel_pcin mba tpr_shadow vnmi flexpriority ept
vpid fsgrsb tsc_adjust bts hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to
  a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 385616 MB
  node 0 free: 385086 MB
  node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387015 MB
  node 1 free: 386548 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal:     791175616 KB
  HugePages_Total:       0
  Hugepagesize:        2048 KB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

(Continued on next page)
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Platform Notes (Continued)

```bash
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
    via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 12 14:48
SPEC is set to: /home/cpu2017
    Filesystem  Type   Size  Used Avail Use% Mounted on
    /dev/sdb1    btrfs  224G   42G  182G  19% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
    Vendor: Cisco Systems Inc
    Product: UCSB-B200-M5
    Serial: FCH22237D2V

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
```

Compiler Version Notes

```
C    | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
---------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
```

(Continued on next page)
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Compiler Version Notes (Continued)

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-----------------------------------------------------------------------------------------------
C++, C, Fortran | 607.cactuBSSN_s(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------------------
Fortran | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------------------
Fortran, C | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
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**Base Compiler Invocation (Continued)**

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

**Base Portability Flags**

- `603.bwaves_s`: `-DSPEC_LP64`
- `607.cactusBSSN_s`: `-DSPEC_LP64`
- `619..hm_s`: `-DSPEC_LP64`
- `621.wrf_s`: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
- `627.cam4_s`: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
- `628.pop2_s`: `-DSPEC_LP64 -DSPEC_CASE_FLAG -assume byterecl`
- `638.imagick_s`: `-DSPEC_LP64`
- `644.nab_s`: `-DSPEC_LP64`
- `649.fotonik3d_s`: `-DSPEC_LP64`
- `654.roms_s`: `-DSPEC_LP64`

**Base Optimization Flags**

**C benchmarks:**
```
xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

**Fortran benchmarks:**
```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs
```

**Benchmarks using both Fortran and C:**
```
xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```

**Benchmarks using Fortran, C, and C++:**
```
xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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Tested with SPEC CPU®2017 v1.1.0 on 2020-04-13 10:31:58-0400.