**SPEC CPU®2017 Integer Rate Result**

**NEC Corporation**

Express5800/R120h-1M (Intel Xeon Silver 4210)

| Spec CPU®2017_int_base = 108 | Spec CPU®2017_int_peak = 112 |

**CPSU2017 License:** 9006  
**Test Sponsor:** NEC Corporation  
**Tested by:** NEC Corporation  
**Software Availability:** Sep-2019  
**Test Date:** Apr-2020  
**Hardware Availability:** Dec-2019  

<table>
<thead>
<tr>
<th>Software Availability</th>
<th>Hardware Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEC BIOS Version U32 v2.22 11/13/2019 released Mar-2020</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>CPU Name: Intel Xeon Silver 4210</td>
</tr>
<tr>
<td>Compiler</td>
<td>Max MHz: 3200</td>
</tr>
<tr>
<td>Compiler</td>
<td>Nominal: 2200</td>
</tr>
<tr>
<td>Compiler</td>
<td>Enabled: 20 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Compiler</td>
<td>Orderable: 1.2 chips</td>
</tr>
<tr>
<td>Compiler</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Compiler</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Compiler</td>
<td>L3: 13.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Compiler</td>
<td>Other: None</td>
</tr>
<tr>
<td>Memory</td>
<td>Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)</td>
</tr>
<tr>
<td>Storage</td>
<td>Storage: 1 x 1 TB SATA, 7200 RPM, RAID 0</td>
</tr>
<tr>
<td>Other</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Spec CPU®2017_int_base (108)</th>
<th>Spec CPU®2017_int_peak (112)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Copies</strong></td>
<td><strong>Copies</strong></td>
</tr>
<tr>
<td>perlbench_r 40</td>
<td>perlbench_r 40</td>
</tr>
<tr>
<td>gcc_r 40</td>
<td>gcc_r 40</td>
</tr>
<tr>
<td>mcf_r 40</td>
<td>mcf_r 40</td>
</tr>
<tr>
<td>omnetpp_r 40</td>
<td>omnetpp_r 40</td>
</tr>
<tr>
<td>xalancbmk_r 40</td>
<td>xalancbmk_r 40</td>
</tr>
<tr>
<td>x264_r 40</td>
<td>x264_r 40</td>
</tr>
<tr>
<td>deepsjeng_r 40</td>
<td>deepsjeng_r 40</td>
</tr>
<tr>
<td>leela_r 40</td>
<td>leela_r 40</td>
</tr>
<tr>
<td>exchange2_r 40</td>
<td>exchange2_r 40</td>
</tr>
<tr>
<td>xz_r 40</td>
<td>xz_r 40</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4210
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 1 TB SATA, 7200 RPM, RAID 0
- **Other:** None
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

NEC Corporation
Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Apr-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
<td>801</td>
<td>79.5</td>
<td>810</td>
<td>78.6</td>
<td>801</td>
<td>79.5</td>
<td>40</td>
<td>697</td>
<td>91.3</td>
<td>698</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
<td>624</td>
<td>90.7</td>
<td>625</td>
<td>90.6</td>
<td>624</td>
<td>90.7</td>
<td>40</td>
<td>557</td>
<td>102</td>
<td>557</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>450</td>
<td>144</td>
<td>448</td>
<td>144</td>
<td>449</td>
<td>144</td>
<td>40</td>
<td>449</td>
<td>144</td>
<td>450</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>40</td>
<td>701</td>
<td>74.9</td>
<td>701</td>
<td>74.8</td>
<td>700</td>
<td>75.0</td>
<td>40</td>
<td>701</td>
<td>74.9</td>
<td>702</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>40</td>
<td>334</td>
<td>127</td>
<td>333</td>
<td>127</td>
<td>333</td>
<td>127</td>
<td>40</td>
<td>314</td>
<td>134</td>
<td>314</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>40</td>
<td>340</td>
<td>206</td>
<td>345</td>
<td>203</td>
<td>343</td>
<td>204</td>
<td>40</td>
<td>326</td>
<td>215</td>
<td>327</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
<td>510</td>
<td>89.9</td>
<td>510</td>
<td>89.8</td>
<td>510</td>
<td>89.9</td>
<td>40</td>
<td>510</td>
<td>89.9</td>
<td>509</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>40</td>
<td>808</td>
<td>82.0</td>
<td>813</td>
<td>81.4</td>
<td>812</td>
<td>81.6</td>
<td>40</td>
<td>808</td>
<td>82.0</td>
<td>813</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
<td>508</td>
<td>206</td>
<td>507</td>
<td>207</td>
<td>508</td>
<td>206</td>
<td>40</td>
<td>508</td>
<td>206</td>
<td>508</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>40</td>
<td>609</td>
<td>70.9</td>
<td>609</td>
<td>70.9</td>
<td>610</td>
<td>70.8</td>
<td>40</td>
<td>609</td>
<td>71.0</td>
<td>608</td>
</tr>
</tbody>
</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

(Continued on next page)
NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Apr-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Thermal Configuration: Maximum Cooling
Workload Profile: General Throughput Compute
Memory Patrol Scrubbing: Disabled
LLC Dead Line Allocation: Disabled
LLC Prefetch: Enabled
Enhanced Processor Performance: Enabled
Workload Profile: Custom
Advanced Memory Protection: Advanced ECC Support
Sub-NUMA Clustering: Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1b1e6e46a485a0011
running on r120h1m Wed Apr 1 07:51:27 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrater®2017_int_base = 108
SPECrater®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Apr-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Platform Notes (Continued)

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2200.000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
   pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
   lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic cpuid nonstop_tsc
   aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
   fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
   xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ebp cat_l3 cdp_l3 invpcid_single
   intel_pmm intel_pt ssbd mba ibrs ibpb stibp ibrs_removed tpr_shadow vmx
   flexpriority vt-d p uprofile tsc_adjust bmi1 hle avx2 smep bmi2 3dnowprefetch erms
   invpcid rtm cqm mpx rd_rset_a avx512f avx512dq rdseed adx smap clflushopt clwb avx512bw
   avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
   dtherm ida arat pin pts pkuv ospe avx512_vnni md_clear spec_ctrl intel_stibp
   flush_lld arch_capabilities

/cache Universität data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
  node 0 size: 196265 MB
  node 0 free: 191655 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
  node 1 size: 196607 MB
  node 1 free: 192039 MB

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

NEC Corporation

Copyright 2017-2020 Standard Performance Evaluation Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrater®2017_int_base = 108
SPECrater®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Test Date: Apr-2020
Tested by: NEC Corporation
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Platform Notes (Continued)

node distances:
node  0  1
0:  10  21
1:  21  10

From /proc/meminfo
MemTotal:       395923400 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*

uname -a:
Linux r120h1m 3.10.0-1062.1.1.el7.x86_64 #1 SMP Tue Aug 13 18:39:59 UTC 2019 x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full retpoline, IBPB

run-level 3 Apr 1 07:45

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      ext4  908G  77G  786G   9% /

From /sys/devices/virtual/dmi/id
BIOS: NEC U32 11/13/2019

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Apr-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Vendor: NEC
Product: Express5800/R120h-1M
Serial: JPN0084094

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x HPE P03050-091 16 GB 2 rank 2933

(End of data from sysinfo program)

Regarding the sysinfo display about the memory speed, the correct configured memory speed is 2400 MT/s. The dmidecode description should be as follows:
24x HPE P03050-091 16 GB 2 rank 2933, configured at 2400

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
(Continued on next page)
### Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>Language</th>
<th>Compilation Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Language</th>
<th>Compilation Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
<td>520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Language</th>
<th>Compilation Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Language</th>
<th>Compilation Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
<td>520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Language</th>
<th>Compilation Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fortran</td>
<td>548.exchange2_r(base, peak)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

NEC Corporation
Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = 112

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
SPEC CPU®2017 Integer Rate Result  
Copyright 2017-2020 Standard Performance Evaluation Corporation

NEC Corporation  
Express5800/R120h-1M (Intel Xeon Silver 4210)  
SPECRate®2017_int_base = 108  
SPECRate®2017_int_peak = 112

CPU2017 License: 9006  
Test Sponsor: NEC Corporation  
Test Date: Apr-2020  
Hardware Availability: Dec-2019  
Tested by: NEC Corporation  
Software Availability: Sep-2019

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc -m64 -std=c11

$icc_r.icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
  icpc -m64

$icpc_r.icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
  ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
  500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
  -fno-strict-overflow
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32
  -lgmalloc

  502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
  -L/usr/local/je5.0.1-32/lib -ljemalloc

  505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4

(Continued on next page)
SPEC CPU®2017 Integer Rate Result  
Copyright 2017-2020 Standard Performance Evaluation Corporation

NEC Corporation  
Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECraten®2017_int_base = 108  
SPECraten®2017_int_peak = 112

Peak Optimization Flags (Continued)

505.mcf_r (continued):
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -fno-alias
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- /usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: basepeak = yes

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevE.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevE.xml
<table>
<thead>
<tr>
<th>NEC Corporation</th>
<th>SPECrate®2017_int_base = 108</th>
</tr>
</thead>
<tbody>
<tr>
<td>Express5800/R120h-1M (Intel Xeon Silver 4210)</td>
<td>SPECrate®2017_int_peak = 112</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Tested by</td>
<td>NEC Corporation</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Apr-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability</td>
<td>Dec-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Sep-2019</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-31 18:51:26-0400.