Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

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**Hardware**

- **CPU Name:** Intel Xeon Gold 5218R
- **Max MHz:** 4000
- **Nominal:** 2100
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 27.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2666)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.1
- **Compiler:** C/C++: Version 19.0.5.281 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.5.281 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPECrater®2017_fp_base = 188
SPECrater®2017_fp_peak = 199

Results Table

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</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/dev/shm/cpu2017/lib/intel64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPECrate®2017_fp_base = 188
SPECrate®2017_fp_peak = 199

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Platform Notes

BIOS settings:
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
Logical Processor enabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled

Sysinfo program /dev/shm/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
running on localhost.localdomain Thu Apr 23 23:04:18 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:

(Continued on next page)
Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate®2017_fp_base = 188
SPECrate®2017_fp_peak = 199

(Continued on next page)

Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 1602.312
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0,4,8,12,16,20,24,28,32,36,40,44,48,52,56,60,64,68,72,76
NUMA node1 CPU(s): 1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61,65,69,73,77
NUMA node2 CPU(s): 2,6,10,14,18,22,26,30,34,38,42,46,50,54,58,62,66,70,74,78
NUMA node3 CPU(s): 3,7,11,15,19,23,27,31,35,39,43,47,51,55,59,63,67,71,75,79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abml 3nowprefetch cpuid_fault epb cat_l3 cdp_l3
invpnc_single intel_pinn ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpnc rtm
cqm mpx rdt_a avx512f avx512dq rdscl edx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts pkur ospke avx512_vnni md_clear flush_l1d
arch_capabilities

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

/node0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPECrate®2017_fp_base = 188
SPECrate®2017_fp_peak = 199

Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: Nov-2019

Platform Notes (Continued)

node 0 size: 95279 MB
node 0 free: 82770 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61 65 69 73 77
node 1 size: 96763 MB
node 1 free: 88958 MB
node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62 66 70 74 78
node 2 size: 96763 MB
node 2 free: 88958 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63 67 71 75 79
node 3 size: 96763 MB
node 3 free: 73182 MB
node distances:
  node 0   1   2   3
  0: 10 21 11 21
  1: 21 10 21 11
  2: 11 21 10 21
  3: 21 11 21 10

From /proc/meminfo
MemTotal: 394824920 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.1 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.1"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
  ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled

(Continued on next page)
Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):  
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):  
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Apr 23 12:56

SPEC is set to: /dev/shm/cpu2017

Filesystem     Type   Size  Used Avail Use% Mounted on
tmpfs          tmpfs  189G   42G  148G  22% /dev/shm

From /sys/devices/virtual/dmi/id
BIOS:    Dell Inc. 2.6.3 02/03/2020
Vendor:  Dell Inc.
Product: PowerEdge M640
Product Family: PowerEdge

Memory:
5x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
4x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
3x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++               | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.5.281 Build 20190815

(Continued on next page)
Dell Inc. PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz) SPECrate®2017_fp_base = 188 SPECrate®2017_fp_peak = 199

CPU2017 License: 55
Test Sponsor: Dell Inc.
Test Date: Apr-2020
Hardware Availability: Feb-2020
Tested by: Dell Inc.
Software Availability: Nov-2019

Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C 511.povray_r(base, peak) 526.blender_r(base, peak)

Intel (R) C++ Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran 507.cactuBSSN_r(base, peak)

Intel (R) C++ Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
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Fortran 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
554.roms_r(base, peak)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
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Fortran, C 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.5.281 Build 20190815
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Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPEC CPU®2017 Floating Point Rate Result

SPECraten®2017_fp_base = 188
SPECraten®2017_fp_peak = 199

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: Nov-2019

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPEC CPU®2017 Floating Point Rate Result

SPECrate®2017_fp_peak = 199
SPECrate®2017_fp_base = 188

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<td>Software Availability:</td>
<td>Nov-2019</td>
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Base Optimization Flags (Continued)

C++ benchmarks (continued):
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both C and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
Dell Inc. PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)

SPECrate®2017_fp_base = 188
SPECrate®2017_fp_peak = 199

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.ibm_r: -m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: -m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

510.parest_r: -m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
503.bwaves_r: -m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

549.fotonik3d_r: basepeak = yes
554.roms_r: -m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs

Benchmarks using both C and C++:

(Continued on next page)
### Dell Inc.

**PowerEdge M640 (Intel Xeon Gold 5218R, 2.10 GHz)**

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<td>Tested by: Dell Inc.</td>
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### Peak Optimization Flags (Continued)

511.povray_r: -m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links: