Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Test Date: May-2020
Hardware Availability: Feb-2020

Tested by: Dell Inc.
Software Availability: Apr-2020

SPECspeed®2017_int_base = 8.76
SPECspeed®2017_int_peak = 8.98

<table>
<thead>
<tr>
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<th>SPECspeed®2017_int_peak = 8.98</th>
</tr>
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<tbody>
<tr>
<td>Threads</td>
<td>600.perlbench_s</td>
</tr>
<tr>
<td>---------</td>
<td>----------------</td>
</tr>
<tr>
<td>Threads</td>
<td>40</td>
</tr>
<tr>
<td>Threads</td>
<td>5.28</td>
</tr>
</tbody>
</table>

**Hardware**

CPU Name: Intel Xeon Silver 4210R
Max MHz: 3200
Nominal: 2400
Enabled: 20 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2400)
Storage: 1 x 480 GB SATA SSD
Other: None

**Software**

OS: Red Hat Enterprise Linux 8.1
Kernel: 4.18.0-147.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 2.6.3 released Feb-2020
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage.
### Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>620.omnetpp_s</td>
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<td>272</td>
<td>6.00</td>
<td>276</td>
<td>5.91</td>
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<td>657.xz_s</td>
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<td>40</td>
<td>334</td>
<td>18.5</td>
<td>335</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 8.76**

**SPECspeed®2017_int_peak = 8.98**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,scatter"

LD_LIBRARY_PATH =
"/root/cpu2017-ic19.1u1/lib/intel64:/root/cpu2017-ic19.1u1/je5.0.1-64"

MALLOC_CONF = "retain:true"

OMP_STACKSIZE = "192M"
Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

| SPECspeed®2017_int_base = 8.76 |
| SPECspeed®2017_int_peak = 8.98 |

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS settings:
Virtualization Technology disabled
DCU Streamer Prefetcher disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor enabled
CPU Interconnect Bus Link Power Management enabled
PCI ASPM L1 Link Power Management enabled

Sysinfo program /root/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e6e46a485a0011
running on localhost.localdomain Thu May 21 21:25:44 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
    2 "physical id"s (chips)
    40 "processors"

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECspeed®2017_int_base = 8.76
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Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              40
On-line CPU(s) list: 0-39
Thread(s) per core:  2
Core(s) per socket:  10
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping:            7
CPU MHz:             1834.557
CPU max MHz:         3200.0000
CPU min MHz:         1000.0000
BogoMIPS:            4800.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            14080K
NUMA node0 CPU(s):   0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38
NUMA node1 CPU(s):   1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgbd rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrpr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abmm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi
flexpriority ept vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdsd adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occump_llc cqm_mmb_total
cqm_mmb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

(Continued on next page)
Dell Inc.

PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

GHz)

SPECspeed®2017_int_base = 8.76
SPECspeed®2017_int_peak = 8.98

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Platform Notes (Continued)

cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
node 0 size: 192073 MB
node 0 free: 171901 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
node 1 size: 193505 MB
node 1 free: 147573 MB
node distances:
node 0 0
 0: 10 21
1: 21 10

From /proc/meminfo
MemTotal:       394833124 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.1 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.1"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
  ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user

(Continued on next page)
**SPEC CPU®2017 Integer Speed Result**

Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

<table>
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</tr>
</tbody>
</table>

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

**Platform Notes (Continued)**

```plaintext
CVE-2017-5715 (Spectre variant 2):
   pointer sanitization
   Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
```

run-level 3 May 15 14:10

SPEC is set to: /root/cpu2017-ic19.1u1

```plaintext
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda2      ext4  439G   24G  394G   6% /
```

From /sys/devices/virtual/dmi/id
   BIOS: Dell Inc. 2.6.3 02/03/2020
   Vendor: Dell Inc.
   Product: PowerEdge M640
   Product Family: PowerEdge

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 5x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
- 4x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
- 3x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
- 4x Not Specified Not Specified

(End of data from sysinfo program)

**Compiler Version Notes**

```
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
         | 625.x264_s(base, peak) 657.xz_s(base, peak)
```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
   NextGen Build 20200304
   Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C       | 600.perlbench_s(peak)
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.1.1.217 Build 20200306
   Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
## Dell Inc.

PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

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### Compiler Version Notes (Continued)

```
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)  
       | 625.x264_s(base, peak) 657.xz_s(base, peak)  

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  

C       | 600.perlbench_s(peak)  

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  

C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)  
       | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)  

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  

Fortran | 648.exchange2_s(base, peak)  

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
```

### Base Compiler Invocation

- **C benchmarks:**  
  - `icc`

- **C++ benchmarks:**  
  - `icpc`

- **Fortran benchmarks:**  
  - `ifort`
**SPEC CPU®2017 Integer Speed Result**

**Dell Inc.**  
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)  

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**Tested by:** Dell Inc.  

**Test Date:** May-2020  
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### Base Portability Flags

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>602.gcc_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>605.mcf_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>620.omnetpp_s: -DSPEC_LP64</td>
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<tr>
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</tr>
<tr>
<td>641.leela_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>648.exchange2_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>657.xz_s: -DSPEC_LP64</td>
</tr>
</tbody>
</table>

### Base Optimization Flags

**C benchmarks:**

```
-m64 -qnextgen -std=c11  
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
-xCORE-AVX2 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops  
-fuse-ld=gold -qopt-mem-layout-trans=4 -fopenmp -DSPEC_OPENMP  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

**C++ benchmarks:**

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto -mfpmath=sse  
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-lqkmalloc
```

**Fortran benchmarks:**

```
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -xCORE-AVX2  
-O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs -align array32byte  
-mbranches-within-32B-boundaries
```

### Peak Compiler Invocation

**C benchmarks:**

```
icc
```

**C++ benchmarks:**

```
icpc
```

*(Continued on next page)*
### Dell Inc.

**PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)**

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#### SPECspeed®2017_int_base = 8.76

#### SPECspeed®2017_int_peak = 8.98

---

### Peak Compiler Invocation (Continued)

Fortran benchmarks:

```plaintext
ifort
```

---

### Peak Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>-DSPEC_LP64, -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>-DSPEC_LP64(*) -DSPEC_LP64</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
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<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

(*) Indicates a portability flag that was found in a non-portability variable.

---

### Peak Optimization Flags

#### C benchmarks:

```plaintext
600.perlbench_s: -W1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64 -qnextgen -std=c11 -fuse-ld=gold
-W1, -plugin-opt=-x86-branches-within-32B-boundaries
-W1, -z, muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -m64 -qnextgen -std=c11
-W1, -plugin-opt=-x86-branches-within-32B-boundaries
-W1, -z, muldefs -xCORE-AVX2 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECspeed®2017_int_base = 8.76
SPECspeed®2017_int_peak = 8.98

Peak Optimization Flags (Continued)

657.xz_s: basepeak = yes
C++ benchmarks:
620.omnetpp_s: basepeak = yes
623.xalancbmk_s: basepeak = yes
631.deepsjeng_s: basepeak = yes
641.leela_s: basepeak = yes
Fortran benchmarks:
648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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