### SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)  

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base = 150</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SPECrate®2017_fp_peak = 156</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 55  
**Test Date:** May-2020  
**Test Sponsor:** Dell Inc.  
**Hardware Availability:** Feb-2020

**Tested by:** Dell Inc.  
**Software Availability:** Apr-2020

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base (150)</th>
<th>SPECrate®2017_fp_peak (156)</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td></td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<td>510.parest_r</td>
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<td>511.povray_r</td>
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<td>519.blm_r</td>
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<tr>
<td>554.roms_r</td>
<td>48</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4214R  
- **Max MHz:** 3500  
- **Nominal:** 2400  
- **Enabled:** 48 cores, 2 chips  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I+D on chip per core  
- **Cache L3:** 16.5 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933V-R, running at 2933)  
- **Storage:** 1 x 1.92 TB SATA SSD  
- **Other:** None  

**Software**

- **OS:** Red Hat Enterprise Linux 8.1  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** No  
- **Firmware:** Version 2.7.7 released May-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  

**Power Management:** BIOS set to prefer performance at the cost of additional power usage
Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

SPECrate®2017_fp_base = 150
SPECrate®2017_fp_peak = 156

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
## General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:
```
sync; echo 3>>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:
```
numactl --interleave=all runcpu <etc>
```

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5


## Platform Notes

BIOS settings:
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor disabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edeb1e6e46a485a0011
running on poweredge-sut-rhel8-1 Sun May 31 06:32:03 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

(Continued on next page)
### SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

**PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)**

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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** May-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** Apr-2020

### Platform Notes (Continued)

From `/proc/cpuinfo`
- **model name**: Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
- 2 "physical id"s (chips)
- 48 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from `/proc/cpuinfo` might not be reliable. Use with caution.)
  - cpu cores : 12
  - siblings : 24
  - physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
  - physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From `lscpu`:
- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **CPU(s)**: 48
- **On-line CPU(s) list**: 0-47
- **Thread(s) per core**: 2
- **Core(s) per socket**: 12
- **Socket(s)**: 2
- **NUMA node(s)**: 4
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 85
- **Model name**: Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
- **Stepping**: 7
- **CPU MHz**: 2917.244
- **CPU max MHz**: 3500.0000
- **CPU min MHz**: 1000.0000
- **BogoMIPS**: 4800.00
- **Virtualization**: VT-x
- **L1d cache**: 32K
- **L1i cache**: 32K
- **L2 cache**: 1024K
- **L3 cache**: 16896K
- **NUMA node0 CPU(s)**: 0,4,8,12,16,20,24,28,32,36,40,44
- **NUMA node1 CPU(s)**: 1,5,9,13,17,21,25,29,33,37,41,45
- **NUMA node2 CPU(s)**: 2,6,10,14,18,22,26,30,34,38,42,46
- **NUMA node3 CPU(s)**: 3,7,11,15,19,23,27,31,35,39,43,47

**Flags:** fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpret pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pchin ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbse tsc_adjust bmi1 hle avx2 smep bmi2 erms invvpid rtm

(Continued on next page)
Platform Notes (Continued)

cqm mpx rdt_a avx512f avx512dq rsseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld
arch_capabilities
/proc/cpuinfo cache data
cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44
node 0 size: 95307 MB
node 0 free: 94755 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45
node 1 size: 96765 MB
node 1 free: 95905 MB
node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46
node 2 size: 96739 MB
node 2 free: 96218 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47
node 3 size: 96764 MB
node 3 free: 96339 MB
node distances:
node 0  1  2  3
  0: 10 21 11 21
  1: 21 10 21 11
  2: 11 21 10 21
  3: 21 11 21 10

From /proc/meminfo
MemTotal: 394831708 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.1 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.1"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)

(Continued on next page)
Dell Inc. PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

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CPU2017 License: 55  
Test Sponsor: Dell Inc.  
Test Date: May-2020

| Test Sponsor: Dell Inc. |
| Hardware Availability: Feb-2020 |
| Software Availability: Apr-2020 |

Platform Notes (Continued)

```bash
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
    Linux poweredge-sut-rhel8-1 4.18.0-147.8.1.el8_1.x86_64 #1 SMP Wed Feb 26 03:08:15 UTC 2020 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- itlb_multihit: Processor vulnerable
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- tsx_async_abort: Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 May 31 00:58 last=5

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
    BIOS: Dell Inc. 2.7.7 05/05/2020
    Vendor: Dell Inc.
    Product: PowerEdge T640
    Product Family: PowerEdge
    Serial: 1234567

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 14x 002C069D002C 18ASF2G72PDZ-2G9E1 16 GB 2 rank 2933
- 2x 00AD00B300AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933
- 4x 00AD00B300AD HMA82GR7CJR8N-XN 16 GB 2 rank 3200
- 4x 00AD069D00AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933

(End of data from sysinfo program)
**Compiler Version Notes**

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)                           |
| 544.nab_r(base, peak)                                         |
| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304                                        |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)                           |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304                                        |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base, peak)                             |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304                                        |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304                                        |
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==============================================================================

==============================================================================
| C++, C          | 511.povray_r(peak)                                                     |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.1.1.217 Build 20200306                                   |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.1.1.217 Build 20200306                                   |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base, peak)                             |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304                                        |
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Compiler Version Notes (Continued)

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-----------------------------------------------

**C++, C** | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

-----------------------------------------------

**C++, C, Fortran** | 507.cactuBSSN_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

-----------------------------------------------

**Fortran** | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
| 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

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-----------------------------------------------

**Fortran, C** | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

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Intel(R) C Compiler for applications running on Intel(R) 64, NextGen Build 20200304
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Fortran, C | 521.wrf_r(peak)

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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

(Continued on next page)
## Dell Inc. PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 150</th>
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<tr>
<td>SPECrate®2017_fp_peak = 156</td>
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### CPU2017 License: 55
- **Test Sponsor:** Dell Inc.
- **Tested by:** Dell Inc.

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### Base Compiler Invocation (Continued)

- **Benchmarks using both Fortran and C:**
  - `ifort icc`

- **Benchmarks using both C and C++:**
  - `icpc icc`

- **Benchmarks using Fortran, C, and C++:**
  - `icpc icc ifort`

### Base Portability Flags

- `503.bwaves_r -DSPEC_LP64`
- `507.cactuBSSN_r -DSPEC_LP64`
- `508.namd_r -DSPEC_LP64`
- `510.parest_r -DSPEC_LP64`
- `511.povray_r -DSPEC_LP64`
- `519.lbm_r -DSPEC_LP64`
- `521.wrf_r -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
- `526.blender_r -DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
- `527.cam4_r -DSPEC_LP64 -DSPEC_CASE_FLAG`
- `538.imagick_r -DSPEC_LP64`
- `544.nab_r -DSPEC_LP64`
- `549.fotonik3d_r -DSPEC_LP64`
- `554.roms_r -DSPEC_LP64`

### Base Optimization Flags

#### C benchmarks:
- `m64 -gnextgen -std=c11`
- `W1, -plugin-opt=-x86-branches-within-32B-boundaries -W1,-z,muldefs`
- `fused-ld-gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse`
- `funroll-loops -qopt-mem-layout-trans=4`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

#### C++ benchmarks:
- `m64 -gnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries`
- `Wl,-z,muldefs -fused-ld-gold -xCORE-AVX2 -Ofast -ffast-math -flto`
- `mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

#### Fortran benchmarks:
- `m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`

(Continued on next page)
Dell Inc.
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**SPEC CPU®2017 Floating Point Rate Result**

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**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- fuse-ld=gold -xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- auto -mbranches-within-32B-boundaries
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both C and C++:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**Peak Compiler Invocation**

C benchmarks:
  icc

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

(Continued on next page)
Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -m64 -qnextgen
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast
-ffast-math -fto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Fortran benchmarks:
503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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Peak Optimization Flags (Continued)

503.bwaves_r (continued):
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
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## Dell Inc.

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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