# SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

<table>
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<tr>
<th>Spec CPU®2017_fp_base</th>
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<tr>
<td>Spec CPU®2017_fp_peak</td>
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**CPU2017 License:** 55  
**Test Date:** May-2020  
**Test Sponsor:** Dell Inc.  
**Hardware Availability:** Feb-2020  
**Tested by:** Dell Inc.  
**Software Availability:** Apr-2020

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<td>554.roms_r</td>
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**Hardware**

- **CPU Name:** Intel Xeon Silver 4210R  
- **Max MHz:** 3200  
- **Nominal:** 2400  
- **Enabled:** 20 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933V-R, running at 2400)  
- **Storage:** 1 x 1.92 TB SATA SSD  
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.1  
  kernel 4.18.0-147.el8.x86_64  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux

- **Parallel:** No  
- **Firmware:** Version 2.7.7 released May-2020  
- **File System:** tmpfs  
- **System State:** Run level 3 (multi-user)  
- **Peak Pointers:** 64-bit  
- **Other:** None  
  jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
Dell Inc. PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz) SPEC CPU® 2017 Floating Point Rate Result

SPECrade®2017_fp_base = 131
SPECrade®2017_fp_peak = 135

Results Table

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "'/mnt/ramdisk/cpu2017-ic19.1u1/lib/intel64:/mnt/ramdisk/cpu2017-ic19.1u1:/je5.0.1-64"
MALLOCC_CONF = "retain:true"
### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numacl i.e.:
umactl --interleave=all runcpu <etc>
Benchmark run from a 225 GB ramdisk created with the cmd; "mount -t tmpfs -o size=225G tmpfs /mnt/ramdisk"
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

### Platform Notes

BIOS settings:
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
Logical Processor enabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /mnt/ramdisk/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edeb1e6e46a485a0011
running on rhel-8-1-sut Mon May 25 18:16:41 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

(Continued on next page)
Dell Inc.  
PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)  

**SPEC CPU®2017 Floating Point Rate Result**

**Dell Inc.**

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  

**SPECrate®2017_fp_base = 131**  
**SPECrate®2017_fp_peak = 135**

---

**Platform Notes (Continued)**

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz  
2 "physical id"s (chips)  
40 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 10  
siblings : 20  
physical 0: cores 0 1 2 3 4 8 9 10 11 12  
physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```plaintext
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 40  
On-line CPU(s) list: 0-39  
Thread(s) per core: 2  
Core(s) per socket: 10  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz  
Stepping: 7  
CPU MHz: 1000.124  
CPU max MHz: 3200.0000  
CPU min MHz: 1000.0000  
BogoMIPS: 4800.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 14080K  
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38  
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dtscache mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl x86op good rdx ibp dtes64 monitoring vt xsave cenx cenv cmov strcmp stremmsintel_pipcd dcatime rcas cmov sxexec efer nmov clflush optmiz86efpu vme pbe sync optmiz87 pdcm dca cssse4_1 cssse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abr mcm cbr mcm abr mcm 3dnowprefetch cpuid_fault epb cat13 cdp_13 invpcid_single intel_pipcd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vmxm flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rsipseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavefs xsavec cqm_llc cqm_occup_llc cqm_mbm_total
```

(Continued on next page)
Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)  

<table>
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<th>SPEC CPU®2017 Floating Point Rate Result</th>
<th>Dell Inc.</th>
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<tr>
<td>SPECrate®2017_fp_peak = 135</td>
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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld arch_capabilities

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
  node 0 size: 192048 MB
  node 0 free: 182749 MB
  node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
  node 1 size: 193531 MB
  node 1 free: 192760 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal:       394833316 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.1 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.1"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
  Linux rhel-8-1-sut 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019 x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected

(Continued on next page)
Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPEC CPU®2017 Floating Point Rate Result

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Dell Inc.

SPECrate®2017_fp_base = 131

SPECrate®2017_fp_peak = 135

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 May 25 12:30 last=5

SPEC is set to: /mnt/ramdisk/cpu2017-ic19.1u1

Filesystem Type Size Used Avail Use% Mounted on
tmpfs tmpfs 150G 4.2G 146G 3% /mnt/ramdisk

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.7 05/04/2020
Vendor: Dell Inc.
Product: PowerEdge R640
Product Family: PowerEdge
Serial: FPFXCH2

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
10x 002C069D002C 18ASF2G72PDZ-2G9E1 16 GB 2 rank 2933
4x 00AD00B300AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933
8x 00AD00B300AD HMA82GR7CJR8N-XN 16 GB 2 rank 3200
2x 00AD063200AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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| C++                | 508.namd_r(base, peak) 510.parest_r(base, peak) |
(Continued on next page)
Dell Inc.
PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECFLOAT®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECRATE®2017_fp_base = 131
SPECRATE®2017_fp_peak = 135

CPU2017 License: 55
Test Sponsor: Dell Inc.
Test Date: May-2020
Tested by: Dell Inc.
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Compiler Version Notes (Continued)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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--------------------------------------------------------------------------
C++, C | 511.povray_r(base) 526.blender_r(base, peak)
--------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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--------------------------------------------------------------------------
C++, C | 511.povray_r(peak)
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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--------------------------------------------------------------------------
C++, C | 511.povray_r(base) 526.blender_r(base, peak)
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
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C++, C | 511.povray_r(peak)
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NextGen Build 20200304
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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(Continued on next page)
Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

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Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
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Test Date: May-2020
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Compiler Version Notes (Continued)

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
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(Continued on next page)
Dell Inc.
PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECrate®2017_fp_base = 131
SPECrate®2017_fp_peak = 135

Compiler Version Notes (Continued)

------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
   64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
   NextGen Build 20200304
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------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
   64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985–2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECrare®2017_fp_base = 131
SPECrare®2017_fp_peak = 135

CPU2017 License: 55
Test Sponsor: Dell Inc.
Test Date: May-2020
Tested by: Dell Inc.
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fused-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrata®2017_fp_base = 131
SPECrata®2017_fp_peak = 135

Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both C and C++:
-m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.

PowerEdge R640 (Intel Xeon Silver 4210R, 2.40 GHz)

| SPECrate®2017_fp_base = 131 |
| SPECrate®2017_fp_peak = 135 |

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r -m64 -gnextgen
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Fortran benchmarks:
503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes
554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:
521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto

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Peak Optimization Flags (Continued)

521.wrf_r (continued):
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml