Lenovo Global Technology
ThinkSystem SR550
(2.40 GHz, Intel Xeon Silver 4210R)

**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology  

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Jun-2020                      |
| **Hardware Availability:**  
Mar-2020                      |
| **Software Availability:**  
Apr-2020                      |  

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**Hardware**

- **CPU Name:** Intel Xeon Silver 4210R
- **Max MHz:** 3200
- **Nominal:** 2400
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 960 GB SATA SSD
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
  Kernel 4.12.14-195-default
- **Compiler:** C/C++: Version 19.1.1.217 of Intel  
  C/C++  
  Compiler for Linux;
- **Compiler for Linux:** Fortran: Version 19.1.1.217 of  
  Intel Fortran
- **Compiler for Linux:** Compiler for Linux
- **Parallel:** No
- **Firmware:** Lenovo BIOS Version TEE155L 2.61 released May-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Lenovo Global Technology
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CPU2017 License: 9017
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Results Table

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Specrate\textsuperscript{\textcircled{2017}} \textsuperscript{int\_base} = 128
Specrate\textsuperscript{\textcircled{2017}} \textsuperscript{int\_peak} = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD\_LIBRARY\_PATH = 
"/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/lib/ia32:/home/cpu2017-1.1.0-ic19.1.1/lib5.0.1-32"
MALLOC\_CONF = "retain:truetrue"
Lenovo Global Technology
ThinkSystem SR550
(2.40 GHz, Intel Xeon Silver 4210R)

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
Memory Power Management set to Automatic
MONITOR/MWAIT set to Enable

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on linux-h3af Sat Jun 6 03:22:54 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
    2 "physical id"s (chips)
    40 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 10
    siblings : 20
    physical 0: cores 0 1 2 3 4 8 9 10 11 12
    physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
### Lenovo Global Technology

**ThinkSystem SR550**  
(2.40 GHz, Intel Xeon Silver 4210R)

<table>
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<tr>
<th>SPECrate®2017_int_base</th>
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<td>Mar-2020</td>
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<tr>
<td>Software Availability</td>
<td>Apr-2020</td>
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**Platform Notes (Continued)**

Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
Address sizes: 46 bits physical, 48 bits virtual  
CPU(s): 40  
On-line CPU(s) list: 0-39  
Thread(s) per core: 2  
Core(s) per socket: 10  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz  
Stepping: 7  
CPU MHz: 2400.000  
CPU max MHz: 3200.0000  
CPU min MHz: 1000.0000  
BogoMIPS: 4800.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 14080K  
NUMA node0 CPU(s): 0-9,20-29  
NUMA node1 CPU(s): 10-19,30-39  
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm abtm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pnip ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmi flexpriority fpt vpid fsqsb tsc_adjust bmi1 hle avx2 smep bmi2 3rms invpcid rtm qm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaves xsaveopt xsaves cvm_llc cvm_occup_llc cvm_mbb_total cvm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 193152 MB
```

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Lenovo Global Technology
ThinkSystem SR550
(2.40 GHz, Intel Xeon Silver 4210R)

SPECrate®2017_int_base = 128
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Jun-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

Platform Notes (Continued)

node 0 free: 192753 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 193501 MB
node 1 free: 192884 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 395933812 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-h3af 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jun 6 03:21

SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 743G 43G 700G 6% /

From /sys/devices/virtual/dmi/id

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR550
(2.40 GHz, Intel Xeon Silver 4210R)

**SPEC CPU®2017 Integer Rate Result**

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Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Compiler Version Notes

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C
| 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) |
| 525.x264_r(base) 557.xz_r(base) |

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C++
| 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) |
| 541.leela_r(base) |

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Fortran
| 548.exchange2_r(base) |

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Lenovo Global Technology  
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**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

---

**SPECrate®2017_int_base = 128**

**SPECrate®2017_int_peak = Not Run**

---

### Base Compiler Invocation

C benchmarks:  
`icc`

C++ benchmarks:  
`icpc`

Fortran benchmarks:  
`ifort`

### Base Portability Flags

500.perlbench_r -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r -DSPEC_LP64  
505.mcf_r -DSPEC_LP64  
520.omnetpp_r -DSPEC_LP64  
523.xalancbmk_r -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r -DSPEC_LP64  
531.deepsjeng_r -DSPEC_LP64  
541.leela_r -DSPEC_LP64  
548.exchange2_r -DSPEC_LP64  
557.xz_r -DSPEC_LP64

### Base Optimization Flags

C benchmarks:  
`-m64 -qnextgen -std=c11`  
`-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`  
`-xCORE-AVX512 -O3 -ffast-math -fto -mfpmath=sse -funroll-loops`  
`-fuse-ld=gold -qopt-mem-layout-trans=4`  
`-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin -lqkmalloc`

C++ benchmarks:  
`-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries`  
`-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -fto -mfpmath=sse`  
`-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4`  
`-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin -lqkmalloc`

Fortran benchmarks:  
`-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`  
`-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4`

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- nostandard-realloc-lhs -align array32byte -auto
- mbranches-within-32B-boundaries
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
- lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-H.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-H.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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Report generated on 2020-06-23 18:08:12 by CPU2017 PDF formatter v6255.
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