Inspur Corporation

Inspur NF5266M5 (Intel Xeon Silver 4215R)

**spec CPU®2017 Floating Point Rate Result**

Copyright 2017-2020 Standard Performance Evaluation Corporation

**SPECrate®2017_fp_base** = 108  
**SPECrate®2017_fp_peak** = 113

**Inspec CPU®2017 License**: 3358  
**Test Sponsor**: Inspur Corporation  
**Tested by**: Inspur Corporation  
**Test Date**: Jun-2020  
**Hardware Availability**: Feb-2020  
**Software Availability**: May-2019

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**Hardware**

**CPU Name**: Intel Xeon Silver 4215R  
**Max MHz**: 4000  
**Nominal**: 3200  
**Enabled**: 16 cores, 2 chips, 2 threads/core  
**Orderable**: 1,2 chips  
**Cache L1**: 32 KB I + 32 KB D on chip per core  
**L2**: 1 MB I+D on chip per core  
**L3**: 11 MB I+D on chip per chip  
**Other**: None  
**Memory**: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
**Storage**: 1 x 10 TB SAS, 7200 RPM, RAID 0  
**Other**: None

**Software**

**OS**: SUSE Linux Enterprise Server 12 SP4  
**Compiler**: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux  
**Parallel**: No  
**Firmware**: Version 3.1.3 released Jul-2019  
**File System**: xfs  
**System State**: Run level 3 (multi-user)  
**Base Pointers**: 64-bit  
**Peak Pointers**: 64-bit  
**Other**: None  
**Power Management**: BIOS and OS set to prefer performance at the cost of additional power usage.
### Results Table

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</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
SCALING_GOVERNOR set to Performance

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/CPU2017/lib/intel64"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3 > /proc/sys/vm/drop_caches`

(Continued on next page)
Inspur Corporation

Inspur NF5266M5 (Intel Xeon Silver 4215R)

SPECrated®2017_fp_base = 108
SPECrated®2017_fp_peak = 113

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: Jun-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

General Notes (Continued)

runcpu command invoked through numactl i.e.: numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
IMC (Integrated memory controller) Interleaving set to 1-way
Sub NUMA Cluster (SNC) set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed16e6e46a485a0011
running on linux-0ot2 Tue Jun 2 07:42:47 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31

(Continued on next page)
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**Platform Notes (Continued)**

- Thread(s) per core: 2
- Core(s) per socket: 8
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
- Stepping: 7
- CPU MHz: 3200.000
- CPU max MHz: 4000.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 6400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 11264K
- NUMA node0 CPU(s): 0-7,16-23
- NUMA node1 CPU(s): 8-15,24-31
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abmlf ndp_prefetch cpuid_fault ebp cat13 cdp13 invpcid_single intel_pmm ssbd mba ibrs ibpb tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erna invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cqm_llc cqm Occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni flush_l1d arch_capabilities

/proccpuinfo cache data

```
 cache size : 11264 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
 available: 2 nodes (0-1) 
 node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23 
 node 0 size: 191997 MB 
 node 0 free: 178036 MB 
 node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31 
 node 1 size: 193324 MB 
 node 1 free: 185968 MB 
 node distances:
 node 0 : 0 1 
 0: 10 21 
```

(Continued on next page)
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Platform Notes (Continued)

From /proc/meminfo
MemTotal: 394570176 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP4

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 4
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP4"
VERSION_ID="12.4"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp4"

uname -a:
Linux linux-0ot2 4.12.14-94.41-default #1 SMP Wed Oct 31 12:25:04 UTC 2018 (3090901)x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jun 1 23:55 last=5

SPEC is set to: /home/CPU2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 xfs 9.1T 38G 9.1T 1% /home

(Continued on next page)
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Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: American Megatrends Inc. 3.1.3 07/04/2019
Vendor: Inspur
Product: NF5266M5
Serial: 219692923

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x Micron 36ASF4G72PZ-2G9E2 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

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<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
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Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
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Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
  icc

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

(Continued on next page)
Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto

(Continued on next page)
## Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
- nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
- m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
- m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

## Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

(Continued on next page)
## Peak Optimization Flags (Continued)

519.lbm_r: 
```
-m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

538.imagick_r: 
```
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```

544.nab_r: Same as 538.imagick_r

### C++ benchmarks:

508.namd_r: 
```
-m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

510.parest_r: 
```
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

### Fortran benchmarks:

503.bwaves_r: 
```
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: 
```
-m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:
```
-m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both C and C++:
```
-m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

526.blender_r: 
```
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```

(Continued on next page)
**Inspur Corporation**

**Inspur NF5266M5 (Intel Xeon Silver 4215R)**

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**Test Sponsor:** Inspur Corporation  
**Tested by:** Inspur Corporation  
**Software Availability:** May-2019

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**Peak Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++:
- `-m64`  
- `-std=c11`  
- `-xCORE-AVX2`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-auto`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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