Lenovo Global Technology
ThinkSystem ST250
(3.80 GHz, Intel Xeon E-2244G)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Jun-2020
Tested by: Lenovo Global Technology
Hardware Availability: Mar-2020

Software
OS: SUSE Linux Enterprise Server 12 SP5 (x86_64)
Kernel 4.12.14-120-default
Compiler: C/C++: Version 19.1.1.217 of Intel
C/C++ Compiler for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Lenovo BIOS Version ISE115D 2.10 released Apr-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage

Hardware
CPU Name: Intel Xeon E-2244G
Max MHz: 4800
Nominal: 3800
Enabled: 4 cores, 1 chip
Orderable: 1 chip
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 256 KB I+D on chip per core
L3: 8 MB I+D on chip per chip
Other: None
Memory: 128 GB (4 x 32 GB 2Rx4 PC4-2666V-E)
Storage: 1 x 960 GB SATA SSD
Other: None

SPEC®2017_fp_base = 27.7
SPECspeed®2017_fp_peak = 28.0

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<th>Threads</th>
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<th>607.cactuBSSN_s</th>
<th>619.ibm_s</th>
<th>621.wrf_s</th>
<th>627.cam4_s</th>
<th>628.pop2_s</th>
<th>638.imagick_s</th>
<th>644.nab_s</th>
<th>649.fotonik3d_s</th>
<th>654.roms_s</th>
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Threads 0-4: SPEC®2017_fp_base (27.7) SPECspeed®2017_fp_peak (28.0)
## Results Table

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<th>Benchmark</th>
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<td>15.5</td>
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**SPECspeed®2017_fp_base = 27.7**

**SPECspeed®2017_fp_peak = 28.0**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/j e5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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General Notes (Continued)

is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
C1 Enhanced Mode set to Enable
Hyper-Threading set to Disable

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed8b166e46a485a0011
running on linux-tzna Tue Jun 23 18:09:02 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) E-2244G CPU @ 3.80GHz
    1 "physical id"s (chips)
    4 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
    siblings : 4
    physical 0: cores 0 1 2 3

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 39 bits physical, 48 bits virtual
CPU(s): 4
On-line CPU(s) list: 0-3
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 158
Model name: Intel(R) Xeon(R) E-2244G CPU @ 3.80GHz
Stepping: 10

(Continued on next page)
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CPU MHz: 3800.000
CPU max MHz: 4800.0000
CPU min MHz: 800.0000
BogoMIPS: 7584.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 256K
L3 cache: 8192K
NUMA node0 CPU(s): 0-3
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer
aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb invpcid_single
pti ssbd ibrs ibpb stibp tpr_shadow vmlinux flexpriority ept vpid fsgsbase tsc_adjust
bmi1 hle avx2 smep bmi2 ets invvpid rtm mpx rdseed adx smap clflushopt intel_pt
xsaveopt xsavec xgetbv1 xsaves dtherm ida arat pln pts hwp hwp_notify hwp_act_window
hwp_epp md_clear flush_l1d

/platform/cpuinfo cache data
 cache size : 8192 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
 available: 1 nodes (0)
 node 0 cpus: 0 1 2 3
 node 0 size: 128867 MB
 node 0 free: 128361 MB
 node distances:
 node 0
 0: 10

From /proc/meminfo
 MemTotal: 131960060 kB
 HugePages_Total: 0
 Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
 SuSE-release:
 SUSE Linux Enterprise Server 12 (x86_64)
 VERSION = 12
 PATCHLEVEL = 5
 # This file is deprecated and will be removed in a future service pack or release.
 # Please check /etc/os-release for details about this release.
 os-release:

(Continued on next page)
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Platform Notes (Continued)

NAME="SLES"
VERSION="12-SP5"
VERSION_ID="12.5"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP5"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp5"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

mitlib_multithit: KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Mitigation: PTE Inversion; VMX: conditional cache flushes, SMT disabled
Microarchitectural Data Sampling: Mitigation: Clear CPU buffers; SMT disabled
CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and ___user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Full generic retpoline, IBPB: conditional, IBRS_FW, RSB filling
tsx_async_abort:
Mitigation: Clear CPU buffers; SMT disabled

run-level 3 Jun 23 18:07

SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1

From /sys/devices/virtual/dmi/id
BIOS: Lenovo -[ISE115D-2.10]- 04/24/2020
Vendor: Lenovo
Product: ThinkSystem ST250 -[7Y45CT00W]-
Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x SK Hynix HMMA4GU7AJR8N-VK 32767 MB 2 rank 2666

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\[ \text{SPECspeed}^{\text{2017_fp_base}} = 27.7 \]
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**Platform Notes (Continued)**

(End of data from sysinfo program)

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**Compiler Version Notes**

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C

\[ 619.lbm_s\text{(base, peak)} 638.imagick_s\text{(base, peak)} \]
\[ 644.nab_s\text{(base, peak)} \]

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C++, C, Fortran

\[ 607.cactuBSSN_s\text{(base, peak)} \]

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Fortran

\[ 603.bwaves_s\text{(base, peak)} 649.fotonik3d_s\text{(base, peak)} \]
\[ 654.roms_s\text{(base, peak)} \]

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Fortran, C

\[ 621.wrf_s\text{(base, peak)} 627.cam4_s\text{(base, peak)} \]
\[ 628.pop2_s\text{(base, peak)} \]

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
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SPECspeed®2017_fp_peak = 28.0
SPECspeed®2017_fp_base = 27.7

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
 -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries

(Continued on next page)
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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-\(\text{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}\)

Benchmarks using both Fortran and C:
-\(\text{-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div}\)
-\(\text{-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp}\)
-\(\text{-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs}\)
-\(\text{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}\)

Benchmarks using Fortran, C, and C++:
-\(\text{-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div}\)
-\(\text{-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp}\)
-\(\text{-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs}\)
-\(\text{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}\)

Peak Compiler Invocation

C benchmarks:
\(\text{icc}\)

Fortran benchmarks:
\(\text{ifort}\)

Benchmarks using both Fortran and C:
\(\text{ifort icc}\)

Benchmarks using Fortran, C, and C++:
\(\text{icpc icc ifort}\)

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
\(\text{619.lbm_s: basepeak = yes}\)

(Continued on next page)
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### Peak Optimization Flags (Continued)

638.imagick_s: basepeak = yes

644.nab_s: -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64.5.0.1/lib -ljemalloc

**Fortran benchmarks:**

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)  
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2  
-03 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64.5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

**Benchmarks using both Fortran and C:**

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)  
-prof-use(pass 2) -ipo -xCORE-AVX2 -03 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP  
-mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/jemalloc64.5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

**Benchmarks using Fortran, C, and C++:**

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-SKL-J.xml](http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-SKL-J.xml)
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<th>Lenovo Global Technology</th>
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<th>Hardware Availability</th>
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**CPU2017 License:** 9017  
**Test Date:** Jun-2020  
**Hardware Availability:** Mar-2020  
**Software Availability:** Apr-2020

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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