# SPEC CPU®2017 Floating Point Rate Result

## Lenovo Global Technology

**ThinkSystem SR650**  
(3.60 GHz, Intel Xeon Gold 6256)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 213</th>
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</table>

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_peak = Not Run</th>
</tr>
</thead>
</table>

**Lenovo Global Technology**  
**Test Date:** Jul-2020  
**Hardware Availability:** Mar-2020  
**Test Sponsor:** Lenovo Global Technology  
**Software Availability:** Apr-2020  

### Hardware

- **CPU Name:** Intel Xeon Gold 6256  
- **Max MHz:** 4500  
- **Nominal:** 3600  
- **Enabled:** 24 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 33 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R)  
- **Storage:** 1 x 800 GB SATA SSD  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
- **Kernel:** 4.12.14-195-default  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++  
- **Compiler for Linux:** Fortran: Version 19.1.1.217 of Intel Fortran  
- **Compiler for Linux:**  
- **Parallel:** No

### Software

- **Firmware:** Lenovo BIOS Version IVE155L 2.61 released May-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

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**Copies**

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## Lenovo Global Technology

ThinkSystem SR650
(3.60 GHz, Intel Xeon Gold 6256)

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**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
    "/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/j
    e5.0.1-64"
MALLOC_CONF = "retain:true"
```

---

**Results Table**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

**SPECrate®2017_fp_base = 213**

**SPECrate®2017_fp_peak = Not Run**
Lenovo Global Technology
ThinkSystem SR650
(3.60 GHz, Intel Xeon Gold 6256)

SPECraten®2017_fp_base = 213
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Jul-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
   sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
   numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
C-States set to Legacy
SNC set to Enable

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbiel6e46a485a0011
running on linux-xyz Mon Jul 13 03:15:01 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Gold 6256 CPU @ 3.60GHz
   2 "physical id"s (chips)
   48 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following
   excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
   cpu cores : 12
   siblings : 24
   physical 0: cores 0 2 3 5 8 11 12 13 17 21 25 26
   physical 1: cores 0 1 3 4 5 8 9 12 13 18 25 27

From lscpu:
   Architecture: x86_64
Lenovo Global Technology
ThinkSystem SR650
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SPECRate®2017_fp_base = 213
SPECRate®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology
Test Date: Jul-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

Platform Notes (Continued)

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6256 CPU @ 3.60GHz
Stepping: 7
CPU MHz: 3600.000
CPU max MHz: 4500.0000
CPU min MHz: 1200.0000
BogoMIPS: 7200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 33792K
NUMA node0 CPU(s): 0-11,24-35
NUMA node1 CPU(s): 12-23,36-47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop tsc cpuid
aerpmperp pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsavex f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cd_p_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmx
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec qcm llc qcm_occup llc qcm_mbb_total
qcm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

/proc/cpuinfo cache data

cache size : 33792 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 386686 MB
node 0 free: 385449 MB

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR650
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CPU2017 License: 9017
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Tested by: Lenovo Global Technology

SPECrater®2017_fp_base = 213
SPECrater®2017_fp_peak = Not Run

Platform Notes (Continued)

node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387036 MB
node 1 free: 386210 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 792292624 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANCE_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-xpyz 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jul 12 21:11
SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 737G 63G 675G 9% /

From /sys/devices/virtual/dmi/id
BIOS: Lenovo -[IVE155L-2.61]- 05/20/2020

(Continued on next page)
Platform Notes (Continued)

Vendor: Lenovo
Product: ThinkSystem SR650 -[7X05RCZ000]-
Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

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<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
   NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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<th>C++</th>
<th>508.namd_r(base) 510.parest_r(base)</th>
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
   NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
   NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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Lenovo Global Technology
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SPECrate®2017_fp_base =  213
SPECrate®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

(Continued on next page)
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SPECrates®2017_fp_base = 213
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CPU2017 License: 9017
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Tested by: Lenovo Global Technology
Test Date: Jul-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-\texttt{L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}

Benchmarks using both Fortran and C:
-\texttt{-m64 -qnextgen -std=c11}
-\texttt{-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs}
-\texttt{-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse}
-\texttt{-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div}
-\texttt{-qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -mbranches-within-32B-boundaries}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}

Benchmarks using both C and C++:
-\texttt{-m64 -qnextgen -std=c11}
-\texttt{-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs}
-\texttt{-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse}
-\texttt{-funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}

Benchmarks using Fortran, C, and C++:
-\texttt{-m64 -qnextgen -std=c11}
-\texttt{-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs}
-\texttt{-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse}
-\texttt{-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div}
-\texttt{-qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -mbranches-within-32B-boundaries}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc}

The flags files that were used to format this result can be browsed at
\url{http://www.spec.org/cpu2017(flags/Intel-ic19.1u1-official-linux64_revA.html}
\url{http://www.spec.org/cpu2017(flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-I.html}

You can also download the XML flags sources by saving the following links:
\url{http://www.spec.org/cpu2017(flags/Intel-ic19.1u1-official-linux64_revA.xml}
\url{http://www.spec.org/cpu2017(flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-I.xml}

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-07-12 15:15:00-0400.
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