SPEC CPU®2017 Integer Rate Result

Inspur Corporation
Inspur NF5180M5 (Intel Xeon Silver 4216)

SPECrate®2017_int_base = 193
SPECrate®2017_int_peak = 199

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation
Hardware Availability: Apr-2019
Software Availability: Apr-2020
Test Date: Jul-2020

Copies

500.perlbench_r 64 151
502.gcc_r 64 154
505.mcf_r 64 176
520.omnetpp_r 64 134
523.xalancbmk_r 64 257
525.x264_r 64 335
531.deepsjeng_r 64 148
541.leela_r 64 136
548.exchange2_r 64 352
557.xz_r 64 117

SPECrater®2017_int_base (193) SPECrater®2017_int_peak (199)

Hardware
CPU Name: Intel Xeon Silver 4216
Max MHz: 3200
Nominal: 2100
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
Storage: 1 x 2TB NVME SSD
Other: None

Software
OS: Red Hat Enterprise Linux release 8.1 (Ootpa)
4.18.0-147.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++
Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran
Compiler Build 20200306 for Linux
Parallel: No
Firmware: Version 4.1.5 released May-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage.
# SPEC CPU® 2017 Integer Rate Result

**Inspur Corporation**

**Inspur NF5180M5 (Intel Xeon Silver 4216)**

<table>
<thead>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
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<th>Copies</th>
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<td>335</td>
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<td>531.deepsjeng_r</td>
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<td>137</td>
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<td>548.exchange2_r</td>
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<tr>
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<td>117</td>
<td>590</td>
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</tr>
</tbody>
</table>

**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

SCALING_GOVERNOR set to Performance

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH =
"/home/CPU2017/lib/intel64:/home/CPU2017/lib/ia32:/home/CPU2017/je5.0.1-32"

MALLOC_CONF = "retain:true"
SPEC CPU®2017 Integer Rate Result

Inspur Corporation
Inspur NF5180M5 (Intel Xeon Silver 4216)

SPECratenet®2017_int_base = 193
SPECratenet®2017_int_peak = 199

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5,
and the system compiler gcc 4.8.5;
sources available from jemalloc.net or

Platform Notes

BIOS configuration:
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
IMC (Integrated memory controller) Interleaving set to 1-way
Sub NUMA Cluster (SNC) set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb6e6e46a485a0011
running on localhost.localdomain Fri Jun 22 07:12:40 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2    "physical id"s (chips)
  64 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

(Continued on next page)
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Inspur Corporation
Inspur NF5180M5 (Intel Xeon Silver 4216)

SPECrate®2017_int_base = 193
SPECrate®2017_int_peak = 199

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Test Date: Jul-2020
Tested by: Inspur Corporation
Hardware Availability: Apr-2019
Software Availability: Apr-2020

Platform Notes (Continued)

    cpu cores : 16
    siblings : 32
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
    physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
    Architecture:        x86_64
    CPU op-mode(s):      32-bit, 64-bit
    Byte Order:          Little Endian
    CPU(s):              64
    On-line CPU(s) list: 0-63
    Thread(s) per core:  2
    Core(s) per socket:  16
    Socket(s):           2
    NUMA node(s):        2
    Vendor ID:           GenuineIntel
    CPU family:          6
    Model:               85
    Model name:          Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
    Stepping:            7
    CPU MHz:             2699.987
    CPU max MHz:         3200.0000
    CPU min MHz:         800.0000
    BogoMIPS:            4200.00
    Virtualization:      VT-x
    L1d cache:           32K
    L1i cache:           32K
    L2 cache:            1024K
    L3 cache:            22528K
    NUMA node0 CPU(s):   0-15,32-47
    NUMA node1 CPU(s):   16-31,48-63
    Flags:               fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic idx pml64idas dtes64 mmu_ende avid tasklibs nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 bs_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vni flexpriority ept cpuid_fault

/proc/cpuinfo cache data
    cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a

(Continued on next page)
**Platform Notes (Continued)**

physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 0 size: 385654 MB
  node 0 free: 385153 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
  node 1 size: 387039 MB
  node 1 free: 386452 MB
  node distances:
  node  0   1
  0:  10  21
  1:  21  10

From /proc/meminfo
  MemTotal:       791238340 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.1 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.1"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
  Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Inspur Corporation**

**Inspur NF5180M5 (Intel Xeon Silver 4216)**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>3358</th>
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<tbody>
<tr>
<td>Test Sponsor:</td>
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<td>Tested by:</td>
<td>Inspur Corporation</td>
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<td><strong>Test Date:</strong></td>
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</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 193**

**SPECrate®2017_int_peak = 199**

---

**Platform Notes (Continued)**

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jun 22 07:11

SPEC is set to: /home/CPU2017

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<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
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</thead>
<tbody>
<tr>
<td>/dev/mapper/rhel-home</td>
<td>xfs</td>
<td>1.8T</td>
<td>86G</td>
<td>1.7T</td>
<td>5%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

**BIOS:** American Megatrends Inc. 4.1.5 05/21/2019  
**Vendor:** Inspur  
**Product:** NF5180M5  
**Serial:** 219243728

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:  
  24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

This system support 12 DIMMs per processor, total 24 DIMMs.  
24 DIMM slots installed with 32 GB DIMM for this run, and running at 2400 due to CPU limitation.

---

**Compiler Version Notes**

```
<table>
<thead>
<tr>
<th>502.gcc_r(peak)</th>
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</thead>
<tbody>
<tr>
<td>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)</td>
</tr>
</tbody>
</table>
```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304

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(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Inspur Corporation**

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**CPU2017 License:** 3358  
**Test Sponsor:** Inspur Corporation  
**Tested by:** Inspur Corporation

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</table>

**Compiler Version Notes (Continued)**

```
C   | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------
C   | 502.gcc_r(peak)
-----------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------
C   | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
       | 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------
C   | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------
C   | 502.gcc_r(peak)
-----------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------
C   | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
       | 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
```

(Continued on next page)
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**SPECraten®2017_int_base = 193**

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### Compiler Version Notes (Continued)

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<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306

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<table>
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<th>C++</th>
<th>520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304

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---

<table>
<thead>
<tr>
<th>Fortran</th>
<th>548.exchange2_r(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306

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---

### Base Compiler Invocation

**C benchmarks:**

- icc

**C++ benchmarks:**

- icpc

**Fortran benchmarks:**

- ifort

---

### Base Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -DSPEC_LP64`

(Continued on next page)
Base Portability Flags (Continued)

505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leea_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc
Inspur Corporation
Inspur NF5180M5 (Intel Xeon Silver 4216)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 193
SPECrate®2017_int_peak = 199

Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

502/gcc_r: -m32
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
-std=gnu89
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries
-Wl, -z, muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
-ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries
-Wl, -z, muldefs -xCORE-AVX512 -flto -O3 -ffast-math

(Continued on next page)
Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4216)

SPECrate®2017_int_base = 193
SPECrate®2017_int_peak = 199

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation
Test Date: Jul-2020
Hardware Availability: Apr-2019
Software Availability: Apr-2020

Peak Optimization Flags (Continued)

525.x264_r (continued):
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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