### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Silver 4215, 2.50GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 96.5</th>
<th>SPECrate®2017_int_peak = Not Run</th>
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**CPU2017 License:** 9019  
**Test Date:** Oct-2020  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  
**Software Availability:** Jun-2020

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<th>Copies</th>
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### Hardware

**CPU Name:** Intel Xeon Silver 4215  
**Max MHz:** 3500  
**Nominal:** 2500  
**Enabled:** 16 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 chips  
**Cache L1:** 32 KB I+ 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 11 MB I+D on chip per chip  
**Other:** None  
**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
**Storage:** 1 x 3.8 TB NVMe SSD  
**Other:** None  
**Power Management:** BIOS set to prefer performance at the cost of additional power usage

### Software

**OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 4.1.2a released Jun-2020  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None
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Results Table

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SPECraten2017_int_base = 96.5
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4215, 2.50GHz)

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General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddie6e46a485a0011
running on linux-hyoc Sat Oct 10 16:19:09 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
 2 "physical id"s (chips)
 32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture:       x86_64
CPU op-mode(s):     32-bit, 64-bit
Byte Order:         Little Endian
Address sizes:      46 bits physical, 48 bits virtual
CPU(s):             32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s):          2

(Continued on next page)
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9019

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Cisco Systems

### Tested by:
Cisco Systems

### Test Date:
Oct-2020

### Hardware Availability:
Apr-2019

### Software Availability:
Jun-2020

### Platform Notes (Continued)

- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
- **Stepping:** 6
- **CPU MHz:** 2500.000
- **CPU max MHz:** 3500.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 5000.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0-7,16-23
- **NUMA node1 CPU(s):** 8-15,24-31

### Flags:
- fpu
- vme
- de
- pse
- tsc
- msr
- pae
- mca
- cmov
- p海
- xsave
- cx16
- xtr\l
- dts
- m\l
- pmx
- sse4_2
- x2apic
- movbe
- popcnt
- tsc_deadline_timer
- aes
- xsave
- lahf_lm
- abm
- bmi1
- hle
- avx2
- smep
- bmi2
- erms
- invpcid
- rtm
- cqm
- mpx
- rdr
- rd\l
- rd\l
- svm
- de
- arch_capabilities

From numactl --hardware

**WARNING:** a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 385459 MB
node 0 free: 384481 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387068 MB
node 1 free: 386389 MB
node distances:
  node 0 1
    0: 10 21
    1: 21 10
```

(Continued on next page)
Platform Notes (Continued)

From /proc/meminfo
    MemTotal: 791068732 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLES"
        VERSION="15-SP1"
        VERSION_ID="15.1"
        PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
    Linux linux-hyoc 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Oct 10 14:53

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/nvme1n1p5 xfs 2.7T 21G 2.7T 1% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. B200M5.4.1.2a.0.0624200115 06/24/2020
    Vendor: Cisco Systems Inc
    Product: UCSB-B200-M5
    Serial: FCH21437BKN

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
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### Platform Notes (Continued)

Memory:  
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

### Compiler Version Notes

```
==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)                  |
|         | 525.x264_r(base) 557.xz_r(base)                                      |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
==============================================================================
| C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)       |
|         | 541.leela_r(base)                                                   |
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
==============================================================================
| Fortran | 548.exchange2_r(base)                                              |
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

### Base Compiler Invocation

- **C benchmarks:**  
  - icc

- **C++ benchmarks:**  
  - icpc

- **Fortran benchmarks:**  
  - ifort
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### Base Portability Flags

- `500.perlbench_r`: `-DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r`: `-DSPEC_LP64`
- `505.mcf_r`: `-DSPEC_LP64`
- `520.omnetpp_r`: `-DSPEC_LP64`
- `523.xalancbmk_r`: `-DSPEC_LP64 -DSPEC_LINUX`
- `525.x264_r`: `-DSPEC_LP64`
- `531.deepsjeng_r`: `-DSPEC_LP64`
- `541.leela_r`: `-DSPEC_LP64`
- `548.exchange2_r`: `-DSPEC_LP64`
- `557.xz_r`: `-DSPEC_LP64`

### Base Optimization Flags

#### C benchmarks:

- `m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

#### C++ benchmarks:

- `m64 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

#### Fortran benchmarks:

- `m64 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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