Inspur Corporation
Inspur NF5288M5 (Intel Xeon Gold 5218R)

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

CPU Name: Intel Xeon Gold 5218R
Max MHz: 4000
Nominal: 2100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
Storage: 1 x 480 TB SATA SSD
Other: None

OS: Red Hat Enterprise Linux release 8.1 (Ootpa)
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
Parallel: No
Firmware: Version 4.1.05 released Jul-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Test Date: Oct-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPEC®2017_fp_peak = Not Run
SPEC®2017_fp_base = 207
**SPEC CPU®2017 Floating Point Rate Result**

**Inspur Corporation**

Inspur NF5288M5 (Intel Xeon Gold 5218R)

---

**SPECrate®2017_fp_base = 207**

**SPECrate®2017_fp_peak = Not Run**

---

**Results Table**

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**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited" SCALING_GOVERNOR set to Performance

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = ":/home/CPU2017/lib/intel64:/home/CPU2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
Inspur Corporation

Inspur NF5288M5 (Intel Xeon Gold 5218R)

SPEC®2017 fp_base = 207
SPEC®2017 fp_peak = Not Run

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: Oct-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
   sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
   numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5,
and the system compiler gcc 4.8.5;
sources available from jemalloc.net or

Platform Notes

BIOS configuration:
   ENERGY_PERF_BIAS_CFG mode set to Performance
   Hardware Prefetch set to Disable
   VT Support set to Disable
   C1E Support set to Disable
   IMC (Integrated memory controller) Interleaving set to 1-way
   Sub NUMA Cluster (SNC) set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbe6e46a485a0011
running on localhost.localdomain Wed Oct 21 09:47:26 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
   2 "physical id"s (chips)
   80 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following
   excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

(Continued on next page)
** SPEC CPU®2017 Floating Point Rate Result **

** Inspur Corporation **

** Inspur NF5288M5 (Intel Xeon Gold 5218R)**

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**CPU2017 License:** 3358  
**Test Sponsor:** Inspur Corporation  
**Tested by:** Inspur Corporation

**Test Date:** Oct-2020  
**Hardware Availability:** Feb-2020  
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---

**Platform Notes (Continued)**

```plaintext
cpu cores : 20  
siblings : 40  
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28  
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From `lscpu`:

```plaintext
Architecture:          x86_64  
CPU op-mode(s):        32-bit, 64-bit  
Byte Order:            Little Endian  
CPU(s):                80  
On-line CPU(s) list:   0-79  
Thread(s) per core:    2  
Core(s) per socket:    20  
Socket(s):             2  
NUMA node(s):          4  
Vendor ID:             GenuineIntel  
CPU family:            6  
Model:                 85  
Model name:            Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz  
Stepping:              7  
CPU MHz:               3680.558  
CPU max MHz:           4000.0000  
CPU min MHz:           800.0000  
BogoMIPS:              4200.00  
Virtualization:       VT-x  
L1d cache:             32K  
L1i cache:             32K  
L2 cache:              1024K  
L3 cache:              28160K  
NUMA node0 CPU(s):     0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56  
NUMA node1 CPU(s):     3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59  
NUMA node2 CPU(s):     20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76  
NUMA node3 CPU(s):     23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79  
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rtde_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsaveopt xsave vsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni md_clear flush_lid arch_capabilities  
```

(Continued on next page)
spec

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Inspur Corporation
Inspur NF5288M5 (Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 207
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CPU2017 License: 3358
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Tested by: Inspur Corporation

Test Date: Oct-2020
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Platform Notes (Continued)

  cache size : 28160 KB

  From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
    node 0 size: 95372 MB
    node 0 free: 88933 MB
    node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
    node 1 size: 96763 MB
    node 1 free: 92517 MB
    node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
    node 2 size: 96738 MB
    node 2 free: 92599 MB
    node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
    node 3 size: 96763 MB
    node 3 free: 92622 MB
    node distances:
      node   0   1   2   3
    0:  10  11  21  21
    1:  11  10  21  21
    2:  21  21  10  11
    3:  21  21  11  10

  From /proc/meminfo
    MemTotal:       394893464 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

  From /etc/*release* /etc/*version*
    os-release:
      NAME="Red Hat Enterprise Linux"
      VERSION="8.1 (Ootpa)"
      ID="rhel"
      ID_LIKE="fedora"
      VERSION_ID="8.1"
      PLATFORM_ID="platform:el8"
      PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
      ANSI_COLOR="0;31"
      redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
      system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
      system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

    uname -a:
      Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
      x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
**Insapur Corporation**

**CPU2017 License:** 3358  
**Test Sponsor:** Insapur Corporation  
**Tested by:** Insapur Corporation

---

**Platform Notes (Continued)**

Kernel self-reported vulnerability status:

- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

---

**run-level 3 Oct 21 02:59**

SPEC is set to: /home/CPU2017  
Filesystem  
| Type   | Size  | Used | Avail | Use% | Mounted on  
|--------|-------|------|-------|------|-------------  
| xfs    | 391G  | 27G  | 364G  | 7%   | /home  

From /sys/devices/virtual/dmi/id  
BIOS: Insapur 4.1.05 07/02/2019  
Vendor: Insapur  
Product: NF5288M5  
Product Family: Not specified  
Serial: 219886866

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.  
Memory:  
- 4x NO DIMM NO DIMM  
- 12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

---

**Compiler Version Notes**

==============================================================================  
| C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)  
|------------------|----------------------------------------  
==============================================================================  
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================  

(Continued on next page)
Compiler Version Notes (Continued)

C++ | 508.namd_r(base) 510.parest_r(base)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C | 511.povray_r(base) 526.blender_r(base)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN_r(base)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
### SPEC CPU®2017 Floating Point Rate Result

**InsPUR Corporation**

**Inspur NF5288M5 (Intel Xeon Gold 5218R)**

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**CPU2017 License:** 3358  
**Test Sponsor:** Inspur Corporation  
**Test Date:** Oct-2020  
**Tested by:** Inspur Corporation  
**Hardware Availability:** Feb-2020  
**Software Availability:** Apr-2020

### Compiler Version Notes (Continued)

NextGen Build 20200304

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### Base Compiler Invocation

- **C benchmarks:**
  - icc

- **C++ benchmarks:**
  - icpc

- **Fortran benchmarks:**
  - ifort

- **Benchmarks using both Fortran and C:**
  - ifort icc

- **Benchmarks using both C and C++:**
  - icpc icc

- **Benchmarks using Fortran, C, and C++:**
  - icpc icc ifort

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
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---

### Base Optimization Flags

C benchmarks:
- m64 -qnextgen -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
- m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- -Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
- m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- -auto -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
- m64 -qnextgen -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- -align array32byte -auto -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both C and C++:
- m64 -qnextgen -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- -align array32byte -auto -mbranches-within-32B-boundaries

(Continued on next page)
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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-10-21 09:47:25-0400.
Originally published on 2020-11-10.