Inspur Corporation

Inspur NE5260M5 (Intel Xeon Gold 5220)

**SPEC CPU®2017 Floating Point Rate Result**

**CPU2017 License:** 3358  
**Test Sponsor:** Inspur Corporation  
**Tested by:** Inspur Corporation

**Test Date:** Oct-2020  
**Hardware Availability:** Apr-2019  
**Software Availability:** Apr-2020

**SPECrate®2017_fp_base = 195**  
**SPECrate®2017_fp_peak = 205**

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<td>554.roms_r 72</td>
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</table>

**Hardware**

**CPU Name:** Intel Xeon Gold 5220  
**Max MHz:** 3900  
**Nominal:** 2200  
**Enabled:** 36 cores, 2 chips, 2 threads/core  
**Orderable:** 1,2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 24.75 MB I+D on chip per chip  
**Other:** None  
**Memory:** 192 GB (12 x 16 GB 2Rx4 PC4-2933Y-R, running at 2666)  
**Storage:** 1 x 4 TB SATA, 7200 RPM  
**Other:** None

**Software**

**OS:** Red Hat Enterprise Linux release 8.2 (Ootpa) 4.18.0-193.el8.x86_64  
**Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux  
**Parallel:** No  
**Firmware:** Version 2.12.0 released Mar-2020  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 64-bit  
**Other:** jemalloc memory allocator V5.0.1  
**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage.
# SPEC CPU®2017 Floating Point Rate Result

## Inspur Corporation

Inspur NE5260M5 (Intel Xeon Gold 5220)

---

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</table>

**SPECrate®2017_fp_base = 195**

**SPECrate®2017_fp_peak = 205**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

SCALING_GOVERNOR set to Performance

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/CPU2017/lib/intel64:/home/CPU2017/je5.0.1-64"
MALLOCONF = "retain:true"
```

---

Page 2

Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/
Inspecr Corporation

Inspur NE5260M5 (Intel Xeon Gold 5220)

**SPECrate®2017_fp_base = 195**
**SPECrate®2017_fp_peak = 205**

<table>
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<th>3358</th>
<th>Test Date:</th>
<th>Oct-2020</th>
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<tr>
<td>Test Sponsor:</td>
<td>Inspur Corporation</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<td>Tested by:</td>
<td>Inspur Corporation</td>
<td>Software Availability:</td>
<td>Apr-2020</td>
</tr>
</tbody>
</table>

---

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3>/proc/sys/vm/drop_caches`
`runcpu command invoked through numactl i.e.:
`numactl --interleave=all runcpu <etc>`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5,
and the system compiler gcc 4.8.5;
sources available from jemalloc.net or

---

**Platform Notes**

BIOS configuration:
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
IMC (Integrated memory controller) Interleaving set to 1-way
Sub NUMA Cluster (SNC) set to Enable
Intel Hyper Threading Technology set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on localhost.localdomain Fri Oct 30 23:47:32 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
  2 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following

(Continued on next page)
Inspur Corporation

Inspur NE5260M5 (Intel Xeon Gold 5220)

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

SPECrate®2017_fp_base = 195
SPECrate®2017_fp_peak = 205

Test Date: Oct-2020
Hardware Availability: Apr-2019
Software Availability: Apr-2020

Platform Notes (Continued)

excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2699.957
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
Flags:
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
  pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
  rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebp cat_l3 cdp_l3 invpcid_single
  intel_pni ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept
  vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
  avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bv avx512vl
  xsavesopt xsaveopt xsetbv1 xsavees cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
  md_clear flush_l1d arch_capabilities

(Continued on next page)
Inspur Corporation

Inspur NE5260M5 (Intel Xeon Gold 5220)

SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 195
SPECrate®2017_fp_peak = 205

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: Oct-2020
Hardware Availability: Apr-2019
Software Availability: Apr-2020

Platform Notes (Continued)

/platform/cpupinfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
  node 0 size: 46950 MB
  node 0 free: 32781 MB
  node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
  node 1 size: 48352 MB
  node 1 free: 34800 MB
  node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
  node 2 size: 48379 MB
  node 2 free: 41060 MB
  node 3 cpus: 21 22 25 26 29 30 34 35 57 58 61 62 65 66 67 70 71
  node 3 size: 48379 MB
  node 3 free: 41329 MB
  node distances:
    node   0   1   2   3
    0:  10  11  21  21
    1:  11  10  21  21
    2:  21  21  10  11
    3:  21  21  11  10

From /proc/meminfo
  MemTotal:       196671632 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release*/etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.2 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.2"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.2 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.2:ga

uname -a:
  Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri Mar 27 14:35:58 UTC 2020
  x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
Platform Notes (Continued)

Kernel self-reported vulnerability status:

<table>
<thead>
<tr>
<th>Vulnerability</th>
<th>Mitigation</th>
</tr>
</thead>
<tbody>
<tr>
<td>itlb_multihit:</td>
<td>KVM: Vulnerable</td>
</tr>
<tr>
<td>CVE-2018-3620 (L1 Terminal Fault):</td>
<td>Not affected</td>
</tr>
<tr>
<td>Microarchitectural Data Sampling:</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2017-5754 (Meltdown):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1):</td>
<td>Mitigation: userscopy/swapgs barriers and __user pointer sanitization</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2):</td>
<td>Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling</td>
</tr>
<tr>
<td>tsx_async_abort:</td>
<td>Mitigation: Clear CPU buffers; SMT vulnerable</td>
</tr>
</tbody>
</table>

run-level 3 Oct 30 14:39

SPEC is set to: /home/CPUC2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 3.5T 63G 3.4T 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Inspur 2.12.0 03/02/2020
Vendor: Inspur
Product: NE5260M5
Product Family: Not specified
Serial: 220658095

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
12x Hynix HMA82GR7JJR8N-WM 16 GB 2 rank 2933
4x NO DIMM NO DIMM

Compiler Version Notes

==============================================================================
<table>
<thead>
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<th>C</th>
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<tr>
<td>519.lbm_r(base, peak) 538.imagick_r(base, peak)</td>
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<td>544.nab_r(base, peak)</td>
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==============================================================================

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304

(Continued on next page)
Inspur Corporation
Inspur NE5260M5 (Intel Xeon Gold 5220)

CPU2017 License: 3358
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Compiler Version Notes (Continued)

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==============================================================================
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C | 511.povray_r(base) 526.blender_r(base, peak)
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C | 511.povray_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C | 511.povray_r(base) 526.blender_r(base, peak)
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
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==============================================================================
C++, C | 511.povray_r(peak)
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**CPU2017 License:** 3358

**Test Sponsor:** Inspur Corporation

**Tested by:** Inspur Corporation

**Test Date:** Oct-2020

**Hardware Availability:** Apr-2019

**Software Availability:** Apr-2020

**Compiler Version Notes (Continued)**

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```plaintext
Fortran, C    | 521.wrf_r(base) 527.cam4_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Inspur NE5260M5 (Intel Xeon Gold 5220)

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Software Availability: Apr-2020

Compiler Version Notes (Continued)

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Intel (R) C Intel (R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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Intel (R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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Fortran, C | 521.wrf_r(peak)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

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**SPEC CPU®2017 Floating Point Rate Result**

**Inspur Corporation**

**Inspur NE5260M5 (Intel Xeon Gold 5220)**

<table>
<thead>
<tr>
<th>CPU2017 License: 3358</th>
<th>Test Date: Oct-2020</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor: Inspur Corporation</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Inspur Corporation</td>
<td>Software Availability: Apr-2020</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 195**

**SPECrate®2017_fp_peak = 205**

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**Base Compiler Invocation (Continued)**

Benchmarks using Fortran, C, and C++:

icpc  icc  ifort

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**Base Portability Flags**

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 527.cam4_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

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**Base Optimization Flags**

**C benchmarks:**

- -m64 -qnextgen -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**C++ benchmarks:**

- -m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- -Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**Fortran benchmarks:**

- -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- -auto -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

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## Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
- `m64 -qnextgen -std=c11`
- `Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`
- `fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse`
- `funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div`
- `qopt-prefetch -ffinite-math-only`
- `qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs`
- `align array32byte -auto -mbranches-within-32B-boundaries`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using both C and C++:
- `m64 -qnextgen -std=c11`
- `Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`
- `fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse`
- `funroll-loops -qopt-mem-layout-trans=4`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using Fortran, C, and C++:
- `m64 -qnextgen -std=c11`
- `Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`
- `fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse`
- `funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div`
- `qopt-prefetch -ffinite-math-only`
- `qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs`
- `align array32byte -auto -mbranches-within-32B-boundaries`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

## Peak Compiler Invocation

C benchmarks:
- `icc`

C++ benchmarks:
- `icpc`

Fortran benchmarks:
- `ifort`

Benchmarks using both Fortran and C:
- `ifort icc`

Benchmarks using both C and C++:
- `icpc icc`
Inspur Corporation
Inspur NE5260M5 (Intel Xeon Gold 5220)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

**SPECrate®2017_fp_peak = 205**
**SPECrate®2017_fp_base = 195**

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Test Date: Oct-2020
Hardware Availability: Apr-2019
Tested by: Inspur Corporation
Software Availability: Apr-2020

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**Peak Compiler Invocation (Continued)**

Benchmarks using Fortran, C, and C++:
icpc icc ifort

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**Peak Portability Flags**

Same as Base Portability Flags

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**Peak Optimization Flags**

C benchmarks:

519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -m64 -qnextgen
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,uldefs -fuse-ld=gold -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Fortran benchmarks:

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,uldefs -fuse-ld=gold -xCORE-AVX2 -O3 -ipo
-no-prec-div -gopt-prefetch -ffinite-math-only
-gopt-multiple-gather-scatter-by-shuffles
-gopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes
554.roms_r: Same as 503.bwaves_r

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Inspur Corporation
Inspur NE5260M5 (Intel Xeon Gold 5220)

SPECcrate®2017_fp_base = 195
SPECcrate®2017_fp_peak = 205

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: Oct-2020
Hardware Availability: Apr-2019
Software Availability: Apr-2020

Peak Optimization Flags (Continued)

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

521.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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