Altos Computing Inc.

BrainSphere R369 F4 (Intel Xeon Gold 5218R)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 218
SPECrate®2017_fp_peak = 231

Altos Computing Inc.

Test Date: Jan-2021
Test Sponsor: Altos Computing Inc.
Tested by: Altos Computing Inc.
Hardware Availability: Nov-2019
Software Availability: Apr-2020

<table>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base (218)</th>
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<td>503.bwaves_r</td>
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<td>507.cactuBSSN_r</td>
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<td>508.namd_r</td>
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**Hardware**

CPU Name: Intel Xeon Gold 5218R
Max MHz: 4000
Nominal: 2100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 1.6 TB SATA SSD
Other: None

**Software**

OS: Red Hat Enterprise Linux release 8.1 (Ootpa) 4.18.0-147.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
Parallel: No
Firmware: Version R11 released Feb-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
## Altos Computing Inc.

BrainSphere R369 F4 (Intel Xeon Gold 5218R)

<table>
<thead>
<tr>
<th>CPU2017 License: 97</th>
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### Results Table

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</tbody>
</table>

**SPECrate®2017_fp_base = 218**

**SPECrate®2017_fp_peak = 231**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
Altos Computing Inc.
BrainSphere R369 F4 (Intel Xeon Gold 5218R)

**SPECrate**<sub>2017_fp_base</sub> = 218  
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<td>Software Availability:</td>
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</tbody>
</table>

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM  
memory using Redhat Enterprise Linux 8.0  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
   `sync; echo 3>/proc/sys/vm/drop_caches`
   `runcpu command invoked through numactl i.e.:`
   `numactl --interleave=all runcpu <etc>`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)  
is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  

**Platform Notes**

BIOS Configuration:  
Power Policy Quick Settings set to Performance  
IMC set to 1-way interleaving  
Sub_NUMA Cluster set to enabled  

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011  
runtime on rhel81 Mon Jan 4 22:52:18 2021  

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
   model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz  
   2 "physical id"s (chips)  
   80 "processors"  
   cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
   cpu cores : 20  
   siblings : 40  
   physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28  
   physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:  
   Architecture:  x86_64

(Continued on next page)
Altos Computing Inc.

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Platform Notes (Continued)

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHZ: 3253.984
CPU max MHZ: 4000.0000
CPU min MHZ: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19,40-59
NUMA node1 CPU(s): 20-39,60-79

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm ablpmlদল 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invvpicid_single intel_pplin ssbd mba ibps ibpm stbpm ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invvpicd rtm cmq mpx rdt_a avx512f avx512dq rseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cmq_llc cmq_occuc_llc cmq_mmm_total cmq_mmm_local dtherm ida arat pln pts hwp hwp_intel_window hwp_egg hwp_pkg_req pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/platform/cpuminfo cache data
  cache size : 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 191845 MB
node 0 free: 171726 MB

(Continued on next page)
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BrainSphere R369 F4 (Intel Xeon Gold 5218R)

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CPU2017 License: 97
Test Sponsor: Altos Computing Inc.
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| Test Date: | Jan-2021 |
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Platform Notes (Continued)

```
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 60 61 62 63 64
65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 1 size: 193502 MB
node 1 free: 175902 MB
node distances:
  node 0 1
    0: 10 21
    1: 21 10
```

From /proc/meminfo
```
MemTotal: 394596436 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*
```
From /proc/meminfo
MemTotal: 394596436 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga
```

```
uname -a:
Linux rhel81 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
```

run-level 3 Jan 4 13:26

SPEC is set to: /home/cpu2017
```

(Continued on next page)
**Altos Computing Inc.**

**BrainSphere R369 F4 (Intel Xeon Gold 5218R)**

**SPECraten®2017_fp_base = 218**

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**Platform Notes (Continued)**

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<td>xfs</td>
<td>1.5T</td>
<td>151G</td>
<td>1.3T</td>
<td>11%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id
- **BIOS:** GIGABYTE R11 02/25/2020
- **Vendor:** ACER
- **Product:** Altos R369 F4
- **Product Family:** Server
- **Serial:** GIH6N4121A0011

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  - 12x NO DIMM NO DIMM
  - 12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

**Compiler Version Notes**

```plaintext
C

| 519.lbm_r (base, peak) 538.imagick_r (base, peak) 544.nab_r (base, peak) |

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++

| 508.namd_r (base, peak) 510.parest_r (base, peak) |

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C

| 511.povray_r (base) 526.blender_r (base, peak) |

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
```

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### Altos Computing Inc.

**BrainSphere R369 F4 (Intel Xeon Gold 5218R)**

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**CPU2017 License:** 97  
**Test Sponsor:** Altos Computing Inc.  
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**Test Date:** Jan-2021  
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### Compiler Version Notes (Continued)

```
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| C++, C          | 511.povray_r(peak) |
------------------------------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, | |
| Version 19.1.1.217 Build 20200306 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
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```

(Continued on next page)
Altos Computing Inc.  
BrainSphere R369 F4 (Intel Xeon Gold 5218R)  

**SPEC CPU®2017 Floating Point Rate Result**

**Compilers**

**Altos Computing Inc.**

**Hardware Availability:** Nov-2019  
**Software Availability:** Apr-2020  
**Test Date:** Jan-2021  
**CPU2017 License:** 97

**Test Sponsor:** Altos Computing Inc.  
**Tested by:** Altos Computing Inc.

**Compiler Version Notes (Continued)**

64, Version 19.1.1.217 Build 20200306  
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Fortran  
| 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
| 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C  
| 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306  
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304  
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Fortran, C  
| 521.wrf_r(peak)

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**SPECrate®2017_fp_base = 218**
**SPECrate®2017_fp_peak = 231**

<table>
<thead>
<tr>
<th>Parameter</th>
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**Compiler Version Notes (Continued)**

Fortran, C  | 521.wrf_r(peak)

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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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**Base Compiler Invocation**

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icc

Benchmarks using both C and C++:
- icpc icc

Benchmarks using Fortran, C, and C++:
- icpc icc ifort

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64

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## SPEC CPU®2017 Floating Point Rate Result

### Altos Computing Inc.

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### SPECrate®2017_fp_base = 218

### SPECrate®2017_fp_peak = 231

#### Base Portability Flags (Continued)

549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

#### Base Optimization Flags

**C benchmarks:**

-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**C++ benchmarks:**

-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**Fortran benchmarks:**

-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**Benchmarks using both Fortran and C:**

-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**Benchmarks using both C and C++:**

-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes

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## Peak Optimization Flags (Continued)

- **538.imagick_r**: basepeak = yes
- **544.nab_r**: basepeak = yes

**C++ benchmarks**:

- **508.namd_r**: basepeak = yes
- **510.parest_r**: -m64 -qnextgen  
  -W1,-plugin-opt=-x86-branches-within-32B-boundaries  
  -W1,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast  
  -ffast-math -flto -mfpmath=sse -funroll-loops  
  -qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib  
  -ljemalloc

**Fortran benchmarks**:

- **503.bwaves_r**: -m64 -W1,-plugin-opt=-x86-branches-within-32B-boundaries  
  -W1,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo  
  -no-prec-div -qopt-prefetch -ffinite-math-only  
  -qopt-multiple-gather-scatter-by-shuffles  
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
  -align array32byte -auto -mbranches-within-32B-boundaries  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

- **549.fotonik3d_r**: basepeak = yes
- **554.roms_r**: Same as 503.bwaves_r

**Benchmarks using both Fortran and C**:

- **521.wrf_r**: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
  -ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
  -qopt-multiple-gather-scatter-by-shuffles  
  -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
  -nostandard-realloc-lhs -align array32byte -auto  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

- **527.cam4_r**: basepeak = yes

**Benchmarks using both C and C++**:

- **511.povray_r**: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
  -ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
  -qopt-multiple-gather-scatter-by-shuffles  
  -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

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## Altos Computing Inc.

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### Peak Optimization Flags (Continued)

- **511.povray_r**:  
  - (continued):
  - `-L/usr/local/jemalloc64-5.0.1/lib` `-ljemalloc`  

- **526.blender_r**: basepeak = yes

- **507.cactuBSSN_r**: basepeak = yes

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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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