SPECCPU®2017 Integer Speed Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.10 GHz, Intel Xeon Gold 5218R)

SPECSpeed®2017_int_base = 8.35
SPECSpeed®2017_int_peak = 8.55

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Jan-2021
Hardware Availability: Aug-2020

Software Availability: Dec-2020

Threads

| Benchmark | 0 | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 | 6.0 | 7.0 | 8.0 | 9.0 | 10.0 | 11.0 | 12.0 | 13.0 | 14.0 | 15.0 | 16.0 | 17.0 | 18.0 | 19.0 | 20.0 |
|-----------|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 600.perlbench_s | 80 |     |     |     |     | 4.98 |     |     |     | 5.85 |     |     |     |     |     |     |     |     |     |     |     |     |
| 602.gcc_s | 80 |     |     |     |     | 8.00 |     |     |     |     | 8.33 |     |     |     |     |     |     |     |     |     |     |     |
| 605.mcf_s | 80 |     |     |     |     | 6.12 |     |     |     |     |     | 14.9 |     |     |     |     |     |     |     |     |     |     |
| 620.omnetpp_s | 80 |     |     |     |     |     | 6.12 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 623.xalancbmk_s | 80 |     |     |     |     |     |     | 10.2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 625.x264_s | 80 |     |     |     |     |     |     |     | 11.7 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 631.deepsjeng_s | 80 |     |     |     |     |     | 4.42 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 641.leela_s | 80 |     |     |     |     |     |     |     |     | 3.57 |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 648.exchange2_s | 80 |     |     |     |     |     |     |     |     |     | 12.3 |     |     |     |     |     |     |     |     |     |     |     |     |
| 657.xz_s | 80 |     |     |     |     |     |     |     |     |     |     | 19.5 |     |     |     |     |     |     |     |     |     |     |     |

SPECspeed®2017_int_base (8.35) SPECspeed®2017_int_peak (8.55)

Hardware

CPU Name: Intel Xeon Gold 5218R
Max MHz: 4000
Nominal: 2100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1.2 (chip)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
Storage: 1 x 480 GB SATA SSD
Other: None

Software

OS: CentOS Linux release 8.3.2011
4.18.0-240.el8.x86_64
Compiler: C/C++; Version 19.1.1.217 of Intel C/C++ Compiler for Linux Build 20200306;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux Build 20200306;
Parallel: Yes
Firmware: Version 3.3 released Feb-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOCONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 2x Intel CacheCade Lake CPU + 384GB RAM memory using Centos 8.2 x86_64

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

(Continued on next page)
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SPECspeed®2017_int_base = 8.35
SPECspeed®2017_int_peak = 8.55

General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the CentOS 8.2 x86_64, and the system compiler gcc 8.3.1 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Sun Jan 31 00:22:55 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
  physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2899.927
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6-10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good ntop制止_cpuid aperfmperf pni pclmulqdq dtses64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pinn ssbd mba ibrs ibpb ibrs_enhanced fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cmp mpg rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/platform/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 90116 MB
node 0 free: 79365 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 92387 MB
node 1 free: 84757 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76

(Continued on next page)
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**SPEC CPU®2017 Integer Speed Result**

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**SPECspeed®2017_int_base = 8.35**
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<th>CPU2017 License: 006042</th>
<th>Test Date: Jan-2021</th>
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<td>Test Sponsor: Netweb Pte Ltd</td>
<td>Hardware Availability: Aug-2020</td>
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<td>Tested by: Tyrone Systems</td>
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</table>

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**Platform Notes (Continued)**

```
node 2 size: 91349 MB
node 2 free: 84594 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 92216 MB
node 3 free: 84641 MB
node distances:
node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10
```

From `/proc/meminfo`

```
MemTotal:       394852092 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

/sbin/tuned-adm active

Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From `/etc/*release* /etc/*version*`

centos-release: CentOS Linux release 8.3.2011
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.3.2011
system-release: CentOS Linux release 8.3.2011
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Test Date: Jan-2021
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Platform Notes (Continued)

Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

run-level 3 Jan 29 16:30
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/cl-home xfs 372G 74G 299G 20% /home

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: Tyrone Camarero DS400TG-48R
Serial: 0123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
4x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.3
BIOS Date: 02/21/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C   | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
    | 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================

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**Compiler Version Notes (Continued)**

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<td>Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304</td>
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</table>

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**Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1**

```
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

---

**Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306**

```
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

---

**Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1**

```
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

---

**Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306**

```
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```
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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -ftlo -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4 -fopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -ftlo -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -xCORE-AVX512
-O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte

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<tr>
<td>Tested by:</td>
<td>Tyrone Systems</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 8.35**  
**SPECspeed®2017_int_peak = 8.55**

### Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- `-mbranches-within-32B-boundaries`

### Peak Compiler Invocation

C benchmarks:
- `icc`

C++ benchmarks:
- `icpc`

Fortran benchmarks:
- `ifort`

### Peak Portability Flags

| Benchmark | Flags                          | (*Indicates a portability flag that was found in a non-portability variable. |
|-----------|--------------------------------|----------------|--------------------------------|
| 600.perlbench_s | -DSPEC_LP64 -DSPEC_LINUX_X64    |                |
| 602.gcc_s      | -DSPEC_LP64(*) -DSPEC_LP64      |                |
| 605.mcf_s      | -DSPEC_LP64                     |                |
| 620.omnetpp_s  | -DSPEC_LP64                     |                |
| 623.xalancbmk_s| -DSPEC_LP64 -DSPEC_LINUX        |                |
| 625.x264_s     | -DSPEC_LP64                     |                |
| 631.deepsjeng_s| -DSPEC_LP64                     |                |
| 641.leela_s    | -DSPEC_LP64                     |                |
| 648.exchange2_s| -DSPEC_LP64                     |                |
| 657.xz_s       | -DSPEC_LP64                     |                |

### Peak Optimization Flags

C benchmarks:
- `600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)`
- `xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -fno-strict-overflow`
- `-mbranches-within-32B-boundaries`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`
SPEC CPU®2017 Integer Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400TG-48R
(2.10 GHz, Intel Xeon Gold 5218R)

SPECspeed®2017_int_base = 8.35
SPECspeed®2017_int_peak = 8.55

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Jan-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

602.gcc_s: -m64 -qnextgen -std=c11 -fuse-ld=gold
-W1,-plugin-opt=-x86-branches-within-32B-boundaries
-W1,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -gopt-mem-layout-trans=4
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: basepeak = yes
625.x264_s: -m64 -qnextgen -std=c11
-W1,-plugin-opt=-x86-branches-within-32B-boundaries
-W1,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math
-fuse-ld=gold -gopt-mem-layout-trans=4 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes
623.xalancbmk_s: basepeak = yes
631.deepsjeng_s: basepeak = yes
641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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