## SPEC CPU®2017 Floating Point Rate Result

### Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400TOG-424RT2
(2.50 GHz, Intel Xeon Gold 6248)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>006042</td>
<td>Feb-2021</td>
<td>Aug-2020</td>
<td>Jun-2020</td>
</tr>
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### SPECrate®2017_fp_base = 239

### SPECrate®2017_fp_peak = 242

| Program       | Copies | 0   | 30  | 60  | 90  | 120 | 150 | 180 | 210 | 240 | 270 | 300 | 330 | 360 | 390 | 420 | 450 | 480 | 510 | 540 | 570 | 600 | 630 | 660 | 690 | 720 | 750 | 780 | 810 | 840 | 870 | 900 | 930 | 960 | 990 | 1020 | 1050 | 1080 | 1110 | 1140 | 1170 | 1200 | 1230 | 1260 | 1290 | 1320 | 1350 | 1380 | 1410 | 1440 | 1470 | 1500 | 1530 | 1560 | 1590 | 1620 | 1650 | 1680 | 1710 | 1740 | 1770 | 1800 | 1830 | 1860 | 1890 | 1920 | 1950 | 1980 | 2010 | 2040 | 2070 | 2100 | 2130 | 2160 | 2190 | 2220 | 2250 | 2280 | 2310 | 2340 | 2370 | 2400 | 2430 | 2460 | 2490 | 2520 | 2550 | 2580 | 2610 | 2640 | 2670 | 2700 | 2730 | 2760 | 2790 | 2820 | 2850 | 2880 | 2910 | 2940 | 2970 | 3000 | 3030 | 3060 | 3090 | 3120 | 3150 | 3180 | 3210 | 3240 | 3270 | 3300 | 3330 | 3360 | 3390 | 3420 | 3450 | 3480 | 3510 | 3540 | 3570 | 3600 | 3630 | 3660 | 3690 | 3720 | 3750 | 3780 | 3810 | 3840 | 3870 | 3900 | 3930 | 3960 | 3990 | 4020 | 4050 | 4080 | 4110 | 4140 | 4170 | 4200 | 4230 | 4260 | 4290 | 4320 | 4350 | 4380 | 4410 | 4440 | 4470 | 4500 | 4530 | 4560 | 4590 | 4620 | 4650 | 4680 | 4710 | 4740 | 4770 | 4800 | 4830 | 4860 | 4890 | 4920 | 4950 | 4980 | 5010 | 5040 | 5070 | 5100 | 5130 | 5160 | 5190 | 5220 | 5250 | 5280 | 5310 | 5340 | 5370 | 5400 | 5430 | 5460 | 5490 | 5520 | 5550 | 5580 | 5610 | 5640 | 5670 | 5700 | 5730 | 5760 | 5790 | 5820 | 5850 | 5880 | 5910 | 5940 | 5970 | 6000 | 6030 | 6060 | 6090 | 6120 | 6150 | 6180 | 6210 | 6240 | 6270 | 6300 | 6330 | 6360 | 6390 | 6420 | 6450 | 6480 | 6510 | 6540 | 6570 | 6600 | 6630 | 6660 | 6690 | 6720 | 6750 | 6780 | 6810 | 6840 | 6870 | 6900 | 6930 | 6960 | 6990 | 7020 | 7050 | 7080 | 7110 |

### Hardware

CPU Name: Intel Xeon Gold 6248
Max MHz: 3900
Nominal: 2500
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1, 2 (chips)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 480 GB SATA SSD
Other: None

### Software

OS: CentOS Linux release 8.2.2004 (Core)
4.18.0-193.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
Firmware: Version 3.3 released Feb-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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</tbody>
</table>

**SPECrate®2017_fp_base = 239**  
**SPECrate®2017_fp_peak = 242**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/jee5.0.1-64"

MALLOC_CONF = "retain:true"
**SPEC CPU®2017 Floating Point Rate Result**

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TOG-424RT2  
(2.50 GHz, Intel Xeon Gold 6248)

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<td>Hardware Availability: Aug-2020</td>
</tr>
<tr>
<td>Tested by: Tyrone Systems</td>
<td>Software Availability: Jun-2020</td>
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</table>

**General Notes**

Binaries compiled on a system with 2x Intel Cascade Lake CPU + 384 GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```bash
sync; echo 3>/proc/sys/vm/drop_caches
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5

**Platform Notes**

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7b080a98a89d4b38e2f1c
running on localhost.localdomain Fri Feb 5 03:06:26 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
- 2 "physical id"s (chips)
- 80 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 20
- siblings : 40
  - physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  - physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

(Continued on next page)
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Platform Notes (Continued)

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
Stepping: 7
CPU MHz: 3554.807
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
apefmpref pni pclmulqdq dtets64 monitor ds_cpl vmx smx est tm ssse3 sdbg fma cx16
xtpr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnni
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local dtherm ida arat pln pts pkup ospke avx512_vnni md_clear flush_l1d
arch_capabilities

/proc/cpuinfo cache data
  cache size : 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 4 nodes (0-3)
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Platform Notes (Continued)

node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 95353 MB
node 0 free: 84556 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 96763 MB
node 1 free: 87684 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 96763 MB
node 2 free: 87145 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 96735 MB
node 3 free: 87732 MB
node distances:
node 0:  10 11 21 21
node 1:  11 10 21 21
node 2:  21 21 10 11
node 3:  21 21 11 10

From /proc/meminfo
MemTotal:       394870504 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  centos-release: CentOS Linux release 8.2.2004 (Core)
  centos-release-upstream: Derived from Red Hat Enterprise Linux 8.2 (Source)
  os-release:
    NAME="CentOS Linux"
    VERSION="8 (Core)"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="8"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="CentOS Linux 8 (Core)"
    ANSI_COLOR="0;31"
  redhat-release: CentOS Linux release 8.2.2004 (Core)
  system-release: CentOS Linux release 8.2.2004 (Core)
  system-release-cpe: cpe:/o:centos:centos:8

uname -a:

(Continued on next page)
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Platform Notes (Continued)

Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri May 8 10:59:10 UTC 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit): KVM: Vulnerable
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2018-3639 (Speculative Store Bypass):
  - Mitigation: usercopy/swapsgs barriers and __user pointer sanitization
- CVE-2017-5753 (Spectre variant 1):
  - Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- CVE-2017-5715 (Spectre variant 2):
  - Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Feb 4 19:20

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: Tyrone Camarero DS400TOG-424RT2
Product Family: SMC X11
Serial: A309085X0907231

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 12x NO DIMM NO DIMM
- 12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

BIOS:
- BIOS Vendor: American Megatrends Inc.
- BIOS Version: 3.3
- BIOS Date: 02/21/2020
- BIOS Revision: 5.14

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Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.libm_r(base, peak) 538.imagick_r(base, peak) |
|                 | 544.nab_r(base, peak) |
==============================================================================
| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
------------------------------------------------------------------------------
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base, peak) |
------------------------------------------------------------------------------
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 |
| NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C          | 511.povray_r(peak) |
------------------------------------------------------------------------------
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| Version 19.1.1.217 Build 20200306 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base, peak) |
------------------------------------------------------------------------------
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
    NextGen Build 20200304
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C++, C, Fortran | 511.povray_r(peak)

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
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C++, C, Fortran | 507.cactuBSSN_r(base, peak)

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
    NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
        554.roms_r(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64,
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
    64, Version 19.1.1.217 Build 20200306
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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TOG-424RT2
(2.50 GHz, Intel Xeon Gold 6248)

SPECrate®2017_fp_base = 239
SPECrate®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
           NextGen Build 20200304
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Compiler Version Notes (Continued)

Fortran, C | 521.wrf_r(peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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           NextGen Build 20200304
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Fortran, C | 521.wrf_r(peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

(Continued on next page)
**Base Compiler Invocation (Continued)**

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

**Base Portability Flags**

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsboxed-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

**Base Optimization Flags**

C benchmarks:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc
```

C++ benchmarks:

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
```
Base Optimization Flags (Continued)

C++ benchmarks (continued):
- mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- m64 -W1, -plugin-opt=-x86-branches-within-32B-boundaries -W1, -z, muldefs
- fuse-lld=gold -xcORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- qopt-mem-layout=4 -nostandard-realloc-lhs -align array32byte
- auto -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib
- ljemalloc

Benchmarks using both Fortran and C:
- m64 -qnextgen -std=c11
- W1, -plugin-opt=-x86-branches-within-32B-boundaries -W1, -z, muldefs
- fuse-lld=gold -xcORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both C and C++:
- m64 -qnextgen -std=c11
- W1, -plugin-opt=-x86-branches-within-32B-boundaries -W1, -z, muldefs
- fuse-lld=gold -xcORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
- ljemalloc

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- W1, -plugin-opt=-x86-branches-within-32B-boundaries -W1, -z, muldefs
- fuse-lld=gold -xcORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

(Continued on next page)
Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes
510.parest_r: -m64 -qnextgen
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -XCORE-AVX512 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc

Fortran benchmarks:

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TOG-424RT2
(2.50 GHz, Intel Xeon Gold 6248)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 239
SPECrate®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Test Date: Feb-2021
Tested by: Tyrone Systems
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Peak Optimization Flags (Continued)

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nomnvec -no-prec-div -ipo
-alignment=v2 -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

549.fotonik3d_r: basepeak = yes
554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml
## SPEC CPU®2017 Floating Point Rate Result

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<tr>
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