### SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TOG-424RT2  
(2.60 GHz, Intel Xeon Gold 6142)

- **SPECrater®2017_int_peak** = 223  
- **SPECrater®2017_int_base** = 215

**Test Sponsor:** Netweb Pte Ltd  
**Test Date:** Feb-2021  
**Hardware Availability:** Aug-2020

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<tr>
<td>xz_r</td>
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<td>130</td>
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</table>

#### Hardware

- **CPU Name:** Intel Xeon Gold 6142  
- **Max MHz:** 3700  
- **Nominal:** 2600  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 (chip)s  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 22 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)  
- **Storage:** 1 x 480 GB SATA SSD  
- **Other:** None

#### Software

- **OS:** CentOS Linux release 8.2.2004 (Core)  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.3 released Feb-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Results Table

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Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"
### General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM memory using Centos 8.2 x86_64

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

### Platform Notes

BIOS Settings:

Power Technology = Custom

Power Performance Tuning = BIOS Controls EPB

ENERGY_PERF_BIAS_CFG mode = Maximum Performance

SNC = Enable

Stale AtoS = Disable

IMC Interleaving = 1-way Interleave

Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Wed Feb 17 10:39:53 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
 2 "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
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Tyrone Camarero DS400TOG-424RT2
(2.60 GHz, Intel Xeon Gold 6142)

SPECrate®2017_int_base = 215
SPECrate®2017_int_peak = 223

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 1588.156
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3, 8-11, 32-35, 40-43
NUMA node1 CPU(s): 4-7, 12-15, 36-39, 44-47
NUMA node2 CPU(s): 16-19, 24-27, 48-51, 56-59
NUMA node3 CPU(s): 20-23, 28-31, 52-55, 60-63
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abml2 abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single pti intel_pni ssbd mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdtd_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_ocppc_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke md_clear flush_l1d

/platform/cpupinfo cache data
  cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
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CPU2017 License: 006042  
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Test Date: Feb-2021  
Hardware Availability: Aug-2020  
Software Availability: Jun-2020

Platform Notes (Continued)

available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43  
node 0 size: 95354 MB  
node 0 free: 94569 MB  
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47  
node 1 size: 96736 MB  
node 1 free: 96377 MB  
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59  
node 2 size: 96764 MB  
node 2 free: 96589 MB  
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63  
node 3 size: 96763 MB  
node 3 free: 96522 MB  
node distances:
  node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10

From /proc/meminfo
  MemTotal:       394874028 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  centos-release: CentOS Linux release 8.2.2004 (Core)
  centos-release-upstream: Derived from Red Hat Enterprise Linux 8.2 (Source)
  os-release:
    NAME="CentOS Linux"
    VERSION="8 (Core)"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="8"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="CentOS Linux 8 (Core)"
    ANSI_COLOR="0;31"
  redhat-release: CentOS Linux release 8.2.2004 (Core)
  system-release: CentOS Linux release 8.2.2004 (Core)
  system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Tested by: Tyrone Systems
Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Platform Notes (Continued)

uname -a:
    Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri May 8 10:59:10 UTC 2020
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Vulnerable
CVE-2018-3620 (L1 Terminal Fault): Mitigation: PTE Inversion
Microarchitectural Data Sampling:
    Mitigation: Clear CPU buffers; SMT vulnerable
CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
    Mitigation: usercopy/swapsgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2):
    Mitigation: Full generic retpoline, IBFB: conditional, IBRS_FW, STIBP: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): No status reported
CVE-2019-11135 (TSX Asynchronous Abort):
    Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Feb 17 10:38

SPEC is set to: /home/cpu2017
From /sys/devices/virtual/dmi/id
    Vendor: Tyrone Systems
    Product: Tyrone Camarero DS400TOG-424RT2
    Product Family: SMC X11
    Serial: A309085X0907231

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
    12x NO DIMM NO DIMM
    12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
    BIOS Vendor: American Megatrends Inc.

(Continued on next page)
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Test Sponsor: Netweb Pte Ltd
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Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Platform Notes (Continued)

BIOS Version: 3.3
BIOS Date: 02/21/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C       | 502.gcc_r(peak)
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
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==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1

(Continued on next page)
## Compiler Version Notes (Continued)

NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Compiler Version Notes (Continued)

Fortran | 548.exchange2_r (base, peak)
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-W1,-plugin-opt=-x86-boundaries-within-32B-boundaries -W1,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compiler_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400T0G-424RT2
(2.60 GHz, Intel Xeon Gold 6142)

SPECrate®2017_int_base = 215
SPECrate®2017_int_peak = 223

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Base Optimization Flags (Continued)

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
-std=gnu89
-XXL,-plugin-opt=-x86-branches-within-32B-boundaries
-XXL,-z,muldefs -fp_profile-use=default.profdata(pass 1)
-XXL,-prof-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass l) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib
-ljemalloc

505.mcf_r: basepeak = yes

520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:

(Continued on next page)
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Peak Optimization Flags (Continued)

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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