SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TOG-424RT2
(2.10 GHz, Intel Xeon Gold 6230)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_peak</th>
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<tbody>
<tr>
<td>SPECrate®2017_fp_base</td>
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Hardware Availability: Aug-2020
Software Availability: Jun-2020

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<tr>
<th>SPECrate®2017_fp_base (224)</th>
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<td>554.roms_r 80</td>
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</table>

Hardware

CPU Name: Intel Xeon Gold 6230
Max MHz: 3900
Nominal: 2100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1.2 (chips)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 480 GB SATA SSD
Other: None

Software

OS: CentOS Linux release 8.2.2004 (Core)
4.18.0-193.el8.x86_64
Compiler: C/C++; Version 19.1.1.217 of Intel C/C++
Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran
Compiler Build 20200306 for Linux
Parallel: No
Firmware: Version 3.3 released Feb-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at
the cost of additional power usage
## Results Table

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</table>

**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"

MALLOC_CONF = "retain:true"
SPEC CPU®2017 Floating Point Rate Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TOG-424RT2
(2.10 GHz, Intel Xeon Gold 6230)

SPECrate®2017_fp_base = 224
SPECrate®2017_fp_peak = 226

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Wed Feb 24 18:59:18 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 20
  siblings : 40
  physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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(Test Sponsor: Netweb Pte Ltd)
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SPECrate®2017_fp_peak = 226

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<tr>
<td>Test Sponsor: Netweb Pte Ltd</td>
<td>Hardware Availability: Aug-2020</td>
</tr>
<tr>
<td>Tested by: Tyrone Systems</td>
<td>Software Availability: Jun-2020</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **CPU(s):** 80
- **On-line CPU(s) list:** 0-79
- **Thread(s) per core:** 2
- **Core(s) per socket:** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
- **Stepping:** 7
- **CPU MHz:** 2718.821
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 4200.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 28160K
- **NUMA node0 CPU(s):** 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
- **NUMA node1 CPU(s):** 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
- **NUMA node2 CPU(s):** 20-22,25,26,30-32,35,36,60-62,65,66,67-72,75,76
- **NUMA node3 CPU(s):** 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
- **Flags:** fpu, vme, vmx, x2apic, movbe, popcnt, tsc_deadline_timer, aes, xsave, avx2, smep, bmi1, lse, avx2, bmi2, avx512f, avx512dq, rdseed, adx, smap, clflushopt, clwb, intel_pt, avx512cd, avx512bw, avx512vl, xsaveopt, xsaves, cqm_llc, cqm_occup_llc, cqm_mbm_total, cqm_mbm_local, dtherm, ida, arat, pln, pts, pku, ospke, avx512_vnni, md_clear, flush_lld, arch_capabilities

/proc/cpuinfo cache data
- **cache size:** 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**

**Tyrone Systems**  
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Tyrone Camarero DS400TOG-424RT2  
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</table>

CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems

**Platform Notes (Continued)**

physical chip.
- available: 4 nodes (0–3)
  - node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
  - node 0 size: 95353 MB
  - node 0 free: 84974 MB
  - node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
  - node 1 size: 96763 MB
  - node 1 free: 87523 MB
  - node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
  - node 2 size: 96735 MB
  - node 2 free: 88186 MB
  - node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
  - node 3 size: 96762 MB
  - node 3 free: 88096 MB
  - node distances:
    - node 0: 10 11 21 21
    - node 1: 11 10 21 21
    - node 2: 21 21 10 11
    - node 3: 21 21 11 10

From /proc/meminfo

- MemTotal: 394870504 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

/sbin/tuned-adm active
- Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

- centos-release: CentOS Linux release 8.2.2004 (Core)
- centos-release-upstream: Derived from Red Hat Enterprise Linux 8.2 (Source)
- os-release:
  - NAME="CentOS Linux"
  - VERSION="8" (Core)"
  - ID="centos"
  - ID_LIKE="rhel fedora"
  - VERSION_ID="8"
  - PLATFORM_ID="platform:el8"
  - PRETTY_NAME="CentOS Linux 8 (Core)"
  - ANSI_COLOR="0;31"
- redhat-release: CentOS Linux release 8.2.2004 (Core)
- system-release: CentOS Linux release 8.2.2004 (Core)
- system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
Platform Notes (Continued)

uname -a:
    Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri May 8 10:59:10 UTC 2020
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):               KVM: Vulnerable
CVE-2018-3620 (L1 Terminal Fault):            Not affected
Microarchitectural Data Sampling:              Not affected
CVE-2017-5754 (Meltdown):                    Mitigation: Speculative Store
    Bypass disabled via prctl and
    seccomp
CVE-2018-3639 (Speculative Store Bypass):     Mitigation: usercopy/swapgs
    barriers and __user pointer
    sanitization
CVE-2017-5753 (Spectre variant 1):            Mitigation: Enhanced IBRS, IBPB:
    conditional, RSB filling
CVE-2017-5715 (Spectre variant 2):            Mitigation: Clear CPU buffers; SMT
    vulnerable
CVE-2020-0543 (Special Register Buffer Data Sampling): No status reported
CVE-2019-11135 (TSX Asynchronous Abort):      Mitigation: Clear CPU buffers; SMT
    vulnerable

run-level 3 Feb 24 10:31

SPEC is set to: /home/cpu2017
    Filesystem          Type  Size  Used Avail Use% Mounted on
    /dev/mapper/cl-home xfs   392G  143G  249G  37% /home

From /sys/devices/virtual/dmi/id
Vendor:         Tyrone Systems
Product:        Tyrone Camarero DS400TOG-424RT2
Product Family: SMC X11
Serial:         A309085X0907231

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
    12x NO DIMM NO DIMM
    12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
BIOS:
    BIOS Vendor:    American Megatrends Inc.
    BIOS Version:  3.3
    BIOS Date:     02/21/2020

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Hardware Availability: Aug-2020
Software Availability: Jun-2020

Platform Notes (Continued)

BIOS Revision: 5.14
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
               | 544.nab_r(base, peak)
==============================================================================
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
==============================================================================
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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==============================================================================
C++, C          | 511.povray_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
**Compiler Version Notes (Continued)**

C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
---------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C          | 511.povray_r(peak)
---------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
  554.roms_r(base, peak)
---------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
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Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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------------------------------------------------------------------
Fortran, C | 521.wrf_r (peak)
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
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------------------------------------------------------------------
Fortran, C | 521.wrf_r (base) 527.cam4_r (base, peak)
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------------------------------------------------------------------
Base Compiler Invocation

C benchmarks:
icc

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TOG-424RT2
(2.10 GHz, Intel Xeon Gold 6230)

SPECrate®2017_fp_base = 224
SPECrate®2017_fp_peak = 226

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Jun-2020

Base Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl, -plugin-opt=-x86-branches-within-32B-boundaries

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Base Optimization Flags (Continued)

C++ benchmarks (continued):
- Wl, -z, muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
- mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- m64 -Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
- fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- auto -mbbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib
- ljemalloc

Benchmarks using both Fortran and C:
- m64 -qnextgen -std=c11
- Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
- fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- -nostandard-realloc-lhs -align array32byte -auto -mbbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both C and C++:
- m64 -qnextgen -std=c11
- Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
- fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- -nostandard-realloc-lhs -align array32byte -auto -mbbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl, -z, muldefs
- fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
- -nostandard-realloc-lhs -align array32byte -auto -mbbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
- icc

(Continued on next page)
Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -m64 -qnextgen
-W1,-plugin-opt=-x86-branches-within-32B-boundaries
-W1,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc

(Continued on next page)
Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-align array32byte -auto -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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