**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 198**

**SPECrate®2017_fp_peak = 201**

<table>
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<tr>
<td>Tested by: Tyrone Systems</td>
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<tr>
<td>554.roms_r</td>
<td>64</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6142
- **Max MHz:** 3700
- **Nominal:** 2600
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 (chips)
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

**Software**

- **OS:** CentOS Linux release 8.3.2011
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++
- **Compiler Build:** 20200306 for Linux;
- **Fortran:** Version 19.1.1.217 of Intel Fortran
- **Compiler Build:** 20200306 for Linux
- **Parallel:** No
- **Firmware:** Version 3.3 released Feb-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.60 GHz, Intel Xeon Gold 6142)

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECRate®2017_fp_base = 198
SPECRate®2017_fp_peak = 201

Results Table

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</table>

SPECRate®2017_fp_base = 198
SPECRate®2017_fp_peak = 201

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCMEM_CONF = "retain: true"
**SPEC CPU®2017 Floating Point Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.60 GHz, Intel Xeon Gold 6142)

**SPECrate®2017_fp_base = 198**
**SPECrate®2017_fp_peak = 201**

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<tr>
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<td>Netweb Pte Ltd</td>
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<td>Tested by:</td>
<td>Tyrone Systems</td>
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<tr>
<td>Hardware Availability:</td>
<td>Aug-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

**General Notes**

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3 > /proc/sys/vm/drop_caches
```
runcpu command invoked through numactl i.e.:
```
numactl --interleave=all runcpu <etc>
```
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5

**Platform Notes**

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Sun Feb 21 00:18:26 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

(Continued on next page)
Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 1582.691
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmprefp pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp l3
invpcid_single pti intel_pstate ssbd mba ibrs ibpb stibp tpr_shadow vnmi flexpriority
ept vpd ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rmep cmpx
rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw
avx512vl xsaveopt xsavec xSAVE vmm擐cq lgicu l1d flush_l1d

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

(Continued on next page)
# SPEC CPU®2017 Floating Point Rate Result

## Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DS400TG-48R**
(2.60 GHz,Intel Xeon Gold 6142)

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**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

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</tbody>
</table>

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**Platform Notes (Continued)**

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 12 33 34 35 40 41 42 43
node 0 size: 91721 MB
node 0 free: 86345 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 92308 MB
node 1 free: 89439 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 93706 MB
node 2 free: 89301 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 93549 MB
node 3 free: 89516 MB
node distances:
node 0: 10 11 21 21
node 1: 11 10 21 21
node 2: 21 21 10 11
node 3: 21 21 11 10
```

---

From `/proc/meminfo`
- MemTotal: 394847488 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

```
/sbin/tuned-adm active
Current active profile: throughput-performance
```

```
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance
```

---

From `/etc/*release` /`etc/*version`
- centos-release: CentOS Linux release 8.3.2011
- centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
- os-release:
  - NAME="CentOS Linux"
  - VERSION="8"
  - ID="centos"
  - ID_LIKE="rhel fedora"
  - VERSION_ID="8"
  - PLATFORM_ID="platform:el8"
  - PRETTY_NAME="CentOS Linux 8"
  - ANSI_COLOR="0;31"
- redhat-release: CentOS Linux release 8.3.2011
- system-release: CentOS Linux release 8.3.2011
- system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.60 GHz, Intel Xeon Gold 6142)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 201

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrater®2017_fp_base = 198
SPECrate®2017_fp_peak = 201

Platform Notes (Continued)

uname -a:
    Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
    KVM: Mitigation: Split huge pages
    MITIGATION: Split huge pages
    CPE-2018-3620 (L1 Terminal Fault):
    Mitigation: PTE Inversion; VMX:
    conditional cache flushes, SMT vulnerable

Microarchitectural Data Sampling:

CVE-2017-5754 (Meltdown):
    Mitigation: PTI
CVE-2018-3639 (Speculative Store Bypass):
    Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5715 (Spectre variant 1):
    Mitigation: usercopy/swaps barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2):
    Mitigation: Full generic retpoline, IBFB: conditional, IBRS_FW, STIBP: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
    Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Feb 20 16:27

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/mapper/cl-home xfs 372G 85G 287G 23% /home

From /sys/devices/virtual/dmi/id
    Vendor: Tyrone Systems
    Product: Tyrone Camarero DS400TG-48R
    Serial: 0123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The dmidecode program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

    Memory:
        4x NO DIMM NO DIMM
        12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.60 GHz, Intel Xeon Gold 6142)

SPECrater®2017_fp_base = 198
SPECrater®2017_fp_peak = 201

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.3
BIOS Date: 02/21/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

C
519.lbm_r(base, peak) 538.imagick_r(base, peak)
544.nab_r(base, peak)

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++
508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C
511.povray_r(base) 526.blender_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
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(Continued on next page)
**Tyrone Systems**  
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Tyrone Camarero DS400TG-48R  
(2.60 GHz, Intel Xeon Gold 6142)

**SPECrate®2017_fp_base = 198**  
**SPECrate®2017_fp_peak = 201**

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Compilers and Version Notes (Continued)

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C++, C  
| 511.povray_r(base) 526.blender_r(base, peak)

Intel (R) C++ Compiler for applications running on Intel (R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel (R) C Compiler for applications running on Intel (R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C  
| 511.povray_r(peak)

Intel (R) C++ Compiler for applications running on Intel (R) 64,  
Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel (R) C Compiler for applications running on Intel (R) 64,  
Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C, Fortran  | 507.cactuBSSN_r(base, peak)

Intel (R) C++ Compiler for applications running on Intel (R) 64,  
Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel (R) C Compiler for applications running on Intel (R) 64,  
Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Fortran  | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)

Intel (R) Fortran Compiler for applications running on Intel (R)  
64, Version 19.1.1.217 Build 20200306  
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(Continued on next page)
Tyrone Systems  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TG-48R  
(2.60 GHz, Intel Xeon Gold 6142)  

SPECraten®2017_fp_base = 198  
SPECraten®2017_fp_peak = 201

CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems

Test Date: Feb-2021  
Hardware Availability: Aug-2020  
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Fortran, C  | 521.wrf_r(base) 527.cam4_r(base, peak)

---

Fortran, C  | 521.wrf_r(peak)

---

Compiler Version Notes (Continued)

Fortran, C  | 521.wrf_r(base) 527.cam4_r(base, peak)

---

Fortran, C  | 521.wrf_r(peak)
## Base Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icc

Benchmarks using both C and C++:
- icpc icc

Benchmarks using Fortran, C, and C++:
- icpc icc ifort

## Base Portability Flags

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<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX -funsigned-char</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

C benchmarks:
- -m64
- -gnextgen  
- -std=c11
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -fuse-ld=gold -xCORE-AVX512  
- -Ofast -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
- -ljemalloc

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TG-48R
(2.60 GHz, Intel Xeon Gold 6142)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 201

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Base Optimization Flags (Continued)

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib
-ljemalloc

Benchmarks using both Fortran and C:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both C and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
## Peak Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icc

Benchmarks using both C and C++:
- icpc icc

Benchmarks using Fortran, C, and C++:
- icpc icc ifort

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:
- 519.lbm_r: basepeak = yes
- 538.imagick_r: basepeak = yes
- 544.nab_r: basepeak = yes

C++ benchmarks:
- 508.namd_r: basepeak = yes

(Continued on next page)
Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -ffinite-math-only
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html
SPEC CPU®2017 Floating Point Rate Result

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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX_revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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