## SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TN-55R  
(2.20 GHz, Intel Xeon Silver 4210)  

<table>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems  

**Test Date:** Feb-2021  
**Hardware Availability:** Aug-2020  
**Software Availability:** Dec-2020

### Hardware

- **CPU Name:** Intel Xeon Silver 4210  
- **Max MHz:** 3200  
- **Nominal:** 2200  
- **Enabled:** 20 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 (chip)  
- **Cache L1:** 32 KB I+ 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
- **Storage:** 1 x 480 GB SATA SSD  
- **Other:** None

### Software

- **OS:** CentOS Linux release 8.3.2011  
- **Kernel:** 4.18.0-240.el8.x86_64  
- **Compiler:** C/C++: Version 19.1.2.254 of Intel C/C++ Compiler Build 20200623 for Linux; Fortran: Version 19.1.2.254 of Intel Fortran Compiler Build 20200623 for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.4 released Nov-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** Jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
SPEC CPU®2017 Integer Rate Result

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CPU2017 License: 006042
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SPECrate®2017_int_base = 122
SPECrate®2017_int_peak = 125

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Results Table

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<td>72.5</td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.2.254 Build 20200623 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.2.254 Build 20200623 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"
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SPECrate®2017_int_base = 122
SPECrate®2017_int_peak = 125

General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM
memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesistem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Thu Feb 25 09:12:16 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
 2 "physical id"s (chips)
 40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
```
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Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 2
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2732.852
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9, 20-29
NUMA node1 CPU(s): 10-19, 30-39
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant-tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmmi ssbd mba ibrs ibpb ibrs_enterprise tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cmip mpg rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512ifc avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cmip_llc cmip_csr cmip_csr cxm_mbb_total cxm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld arch_capabilities

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)

(Continued on next page)
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**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

**Test Date:** Feb-2021  
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**Software Availability:** Dec-2020

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**Platform Notes (Continued)**

<table>
<thead>
<tr>
<th>Node 0 CPUs</th>
<th>Node 0 Size</th>
<th>Node 0 Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29</td>
<td>185188 MB</td>
<td>183462 MB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Node 1 CPUs</th>
<th>Node 1 Size</th>
<th>Node 1 Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39</td>
<td>186668 MB</td>
<td>192841 MB</td>
</tr>
</tbody>
</table>

**From /proc/meminfo**

- MemTotal: 394870792 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

**/sbin/tuned-adm active**

- Current active profile: throughput-performance

**/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor** has performance

**From /etc/*release*/etc/*version**

- centos-release: CentOS Linux release 8.3.2011
- centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
- os-release:
  - NAME="CentOS Linux"
  - VERSION="8"
  - ID="centos"
  - ID_LIKE="rhel fedora"
  - VERSION_ID="8"
  - PLATFORM_ID="platform:e18"
  - PRETTY_NAME="CentOS Linux 8"
  - ANSI_COLOR="0;31"

**Kernel self-reported vulnerability status:**

- CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected

(Continued on next page)
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Platform Notes (Continued)

CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

run-level 3 Feb 25 02:33
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/cl-home xfs 372G 5.8G 366G 2% /home

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: X11DPi-N(T)
Product Family: SMC X11
Serial: 123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.4
BIOS Date: 11/23/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 502.gcc_r(peak) |
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen

(Continued on next page)
**Tyrone Systems**  
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**Compiler Version Notes (Continued)**

**Build 20200304**  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
*icc (NextGen): command line warning #10006: ignoring unknown option*  
'-i_version=19.1.2.254' [-Woption-ignored]

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<table>
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<tbody>
<tr>
<td></td>
<td>525.x264_r(base, peak) 557.xz_r(base)</td>
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
*icc (NextGen): command line warning #10006: ignoring unknown option*  
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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**SPECrate®2017_int_base = 122**  
**SPECrate®2017_int_peak = 125**

### Compiler Version Notes (Continued)

```plaintext
C       | 500.perlbench_r(peak) 557.xz_r(peak)  
----------------------------------------------  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.2.254 Build 20200623  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
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| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)  
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
icpc (NextGen): command line warning #10006: ignoring unknown option  
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(Continued on next page)
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Software Availability: Dec-2020

Compiler Version Notes (Continued)

Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.2.254 Build 20200623
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Base CompilerInvocation

C benchmarks:
ic
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -mnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin
-lqkmalloc

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Tyrone Systems

*(Test Sponsor: Netweb Pte Ltd)*

Tyrone Camarero DS400TN-55R  
(2.20 GHz, Intel Xeon Silver 4210)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
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<td>Test Sponsor:</td>
<td>Netweb Pte Ltd</td>
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<td>Tested by:</td>
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<table>
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<tr>
<th>SPECrate®2017_int_peak = 125</th>
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</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base = 122</td>
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</tbody>
</table>

### Base Optimization Flags (Continued)

```
C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin
-lqkmalloc
```

### Peak Compiler Invocation

```
C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort
```

### Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```
## SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Works Sponsor: Netweb Pte Ltd)  
**Tyrone Camarero DS400TN-55R**  
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**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems  
**Test Date:** Feb-2021  
**Hardware Availability:** Aug-2020  
**Software Availability:** Dec-2020

### Peak Optimization Flags

**C benchmarks:**

- 500.perlbench_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)`  
- `-xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4 -fno-strict-overflow`  
- `-mbranches-within-32B-boundaries`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin -lqkmalloc`  
- 502.gcc_r: `-m32`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/ia32_lin -std=gnu89`  
- `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries`  
- `-Wl,-z,muldefs -fprofile-generate(pass 1)`  
- `-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto -Ofast(pass 1) -O3 -ffast-math -qnextgen -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc`  
- 505.mcf_r: `basepeak = yes`  
- 525.x264_r: `-m64 -qnextgen -std=c11`  
- `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries`  
- `-Wl,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math -fno-alias`  
- `-qopt-mem-layout-trans=4 -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin -lqkmalloc`  
- 557.xz_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.2.254/linux/compiler/lib/intel64_lin -lqkmalloc`

**C++ benchmarks:**

- 520.omnetpp_r: `basepeak = yes`  
- 523.xalancbmk_r: `basepeak = yes`  
- 531.deepsjeng_r: `basepeak = yes`  
- 541.leela_r: `basepeak = yes`

**Fortran benchmarks:**

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
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SPECrate®2017_int_base = 122
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CPU2017 License: 006042
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Peak Optimization Flags (Continued)

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml

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