## SPEC CPU®2017 Floating Point Rate Result

**Cpu2017 License**: 006042  
**Test Sponsor**: Netweb Pte Ltd  
**Tested by**: Tyrone Systems  
**Test Date**: Feb-2021  
**Hardware Availability**: Aug-2020  
**Software Availability**: Dec-2020

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<tr>
<th>Test</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tr>
<td>503.bwaves_r</td>
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<td>127</td>
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<tr>
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<tr>
<td>554.roms_r</td>
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<td>127</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name**: Intel Xeon Silver 4210  
- **Max MHz**: 3200  
- **Nominal**: 2200  
- **Enabled**: 20 cores, 2 chips, 2 threads/core  
- **Orderable**: 1,2 (chip)s  
- **Cache L1**: 32 KB I + 32 KB D on chip per core  
- **Cache L2**: 1 MB I+D on chip per core  
- **Cache L3**: 13.75 MB I+D on chip per chip  
- **Other**: None  
- **Memory**: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
- **Storage**: 1 x 480 GB SATA SSD  
- **Other**: None

### Software

- **OS**: CentOS Linux release 8.3.2011  
- **Kernel**: 4.18.0-240.el8.x86_64  
- **Compiler**: C/C++: Version 19.1.2.254 of Intel C/C++ Compiler Build 20200623 for Linux; Fortran: Version 19.1.2.254 of Intel Fortran Compiler Build 20200623 for Linux  
- **Parallel**: No  
- **Firmware**: Version 3.4 released Nov-2020  
- **File System**: xfs  
- **System State**: Run level 3 (multi-user)  
- **Base Pointers**: 64-bit  
- **Peak Pointers**: 64-bit  
- **Other**: jemalloc memory allocator V5.0.1  
- **Power Management**: BIOS set to prefer performance at the cost of additional power usage.
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TN-55R
(2.20 GHz, Intel Xeon Silver 4210)

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Results Table

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<td>1050</td>
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</table>

SPECrate®2017_fp_base = 125
SPECrate®2017_fp_peak = 127

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM
memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

(Continued on next page)
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**Tyrone Camarero DS400TN-55R**  
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### General Notes (Continued)

- The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

### Platform Notes

**BIOS Settings:**
- Power Technology = Custom
- Power Performance Tuning = BIOS Controls EPB
- ENERGY_PERF_BIAS_CFG mode = Maximum Performance
- SNC = Enable
- Stale AtoS = Disable
- IMC Interleaving = 1-way Interleave
- Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c  
running on localhost.localdomain Thu Feb 25 17:53:05 2021

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 10
  siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian

(Continued on next page)
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Platform Notes (Continued)

CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2738.747
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9, 20-29
NUMA node1 CPU(s): 10-19, 30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pinn ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid ept_ad fs_dbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cmq mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts kpu ospke avx512_vnni md_clear
flush_lld arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 185188 MB
node 0 free: 171688 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 186668 MB
node 1 free: 184338 MB

(Continued on next page)
Platform Notes (Continued)

node distances:
node  0  1
  0:  10  21
  1:  21  10

From /proc/meminfo
  MemTotal:       394870792 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  centos-release: CentOS Linux release 8.3.2011
  centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
  os-release:
    NAME="CentOS Linux"
    VERSION="8"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="8"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="CentOS Linux 8"
    ANSI_COLOR="0;31"
  redhat-release: CentOS Linux release 8.3.2011
  system-release: CentOS Linux release 8.3.2011
  system-release-cpe: cpe:/o:centos:centos:8

uname -a:
  Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
KVM: Mitigation: Split huge pages
Not affected

CVE-2018-3620 (L1 Terminal Fault):
Not affected

Microarchitectural Data Sampling:
Not affected

CVE-2017-5754 (Meltdown):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2018-3639 (Speculative Store Bypass):
Mitigation: usercopy/swaps barriers and __user pointer

CVE-2017-5753 (Spectre variant 1):

(Continued on next page)
Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

run-level 3 Feb 25 02:33

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/cl-home xfs 372G 26G 347G 7% /home

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: X11DPi-N(T)
Product Family: SMC X11
Serial: 123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.4
BIOS Date: 11/23/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

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<table>
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<th>C</th>
<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
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<tr>
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<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
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<td>icc (NextGen): command line warning #10006: ignoring unknown option</td>
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<td>'-i_version=19.1.2.254' [-Woption-ignored]</td>
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Fortran  |  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.2.254 Build 20200623
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Intel(R) C Compiler for applications running on Intel(R) 64,
Version 19.1.2.254 Build 20200623
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## SPEC CPU®2017 Floating Point Rate Result

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 125**

**SPECrate®2017_fp_peak = 127**

### Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DS400TN-55R**

(2.20 GHz, Intel Xeon Silver 4210)

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### Base Compiler Invocation

- **C benchmarks:**
  - icc

- **C++ benchmarks:**
  - icpc

- **Fortran benchmarks:**
  - ifort

- **Benchmarks using both Fortran and C:**
  - ifort icc

- **Benchmarks using both C and C++:**
  - icpc icc

- **Benchmarks using Fortran, C, and C++:**
  - icpc icc ifort

### Base Portability Flags

- 503. bwaves_r: -DSPEC_LP64
- 507. cactuBSSN_r: -DSPEC_LP64
- 508. namd_r: -DSPEC_LP64
- 510. parest_r: -DSPEC_LP64
- 511. povray_r: -DSPEC_LP64
- 519. IBM_r: -DSPEC_LP64
- 521. wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526. blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527. cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538. imagick_r: -DSPEC_LP64
- 544. nab_r: -DSPEC_LP64
- 549. fotonik3d_r: -DSPEC_LP64
- 554. roms_r: -DSPEC_LP64

### Base Optimization Flags

- **C benchmarks:**
  - -m64
  - -mnextgen
  - -std=c11
  - -Wl,-plugin-opt=x86-branches-within-32B-boundaries
  - -Wl,-z,muldefs
  - -xCORE-AVX512
  - -Ofast
  - -ffast-math
  - -fno-printf
  - -mfpmath=sse
  - -funroll-loops
  - -qopt-mem-layout-trans=4
  - -L/usr/local/je5.0.1-64/lib
  - -ljemalloc

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C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib
-ljemalloc

Benchmarks using both Fortran and C:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both C and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

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Peak Compiler Invocation (Continued)

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

Benchmarks using both C and C++:
  icpc icc

Benchmarks using Fortran, C, and C++:
  icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
  519.lbm_r: basepeak = yes
  538.imagick_r: basepeak = yes
  544.nab_r: basepeak = yes

C++ benchmarks:
  508.namd_r: basepeak = yes
  510.parest_r: -m64 -qnextgen
    -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
    -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
    -mfpmath=sse -funroll-loops -gopt-mem-layout-trans=4
    -L/usr/local/jemalloc -ljemalloc

Fortran benchmarks:

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#### Peak Optimization Flags (Continued)

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div  
-qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-nostandard-realloc-lhs -align array32byte -auto  
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml  
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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