Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 387</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** May-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Mar-2021

| Copies | 0 | 50.0 | 100 | 150 | 200 | 250 | 300 | 350 | 400 | 450 | 500 | 550 | 600 | 650 | 700 | 750 | 800 | 850 | 900 | 950 | 1000 | 1050 | 1100 |
|--------|---|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 503.bwaves_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 507.cactuBSSN_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 508.namd_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 510.parest_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 511.povray_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 519.lbm_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 521.wrf_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 526.blender_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 527.cam4_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 538.imagick_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 544.nab_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 549.fotonik3d_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| 554.roms_r | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 | 112 |

---

**Hardware**

CPU Name: Intel Xeon Gold 6348  
Max MHz: 3500  
Nominal: 2600  
Enabled: 56 cores, 2 chips, 2 threads/core  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 48 KB D on chip per core  
L2: 1.25 MB I+D on chip per core  
L3: 42 MB I+D on chip per chip  
Other: None  
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)  
Storage: 1 x 300 GB 15K SAS HDD  
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP2  
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
Parallel: No  
Firmware: Version 4.2.1b released May-2021  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: Not Applicable  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
## SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

### SPECrate®2017_fp_base = 387

### SPECrate®2017_fp_peak = Not Run

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</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
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<td>Software Availability:</td>
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---

### Results Table

<table>
<thead>
<tr>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>1556</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<td>266</td>
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<td>530</td>
<td>266</td>
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<td>508.namd_r</td>
<td>112</td>
<td>340</td>
<td>313</td>
<td>340</td>
<td>313</td>
<td>342</td>
<td>311</td>
</tr>
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<td>342</td>
<td>732</td>
<td>343</td>
<td>749</td>
<td>335</td>
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<td>411</td>
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<td>1080</td>
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<td>1070</td>
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<td>1050</td>
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<td>270</td>
<td>698</td>
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<td>268</td>
<td>704</td>
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<td>1909</td>
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<td>1909</td>
<td>229</td>
<td>1909</td>
<td>229</td>
</tr>
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<td>554.roms_r</td>
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<td>154</td>
<td>1151</td>
<td>155</td>
<td>1155</td>
<td>154</td>
</tr>
</tbody>
</table>

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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- `LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"`
- `MALLOC_CONF = "retain:true"`

---

### General Notes

Binaries compiled on a system with 1x Intel Core i9–7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

---

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 387
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

General Notes (Continued)

sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numacll i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c running on localhost Fri May 21 23:53:36 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
  2 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 28
  siblings : 56
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

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</table>

Test Date: May-2021
Hardware Availability: Apr-2021
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Platform Notes (Continued)

CPU(s): 112
On-line CPU(s) list: 0-111
Thread per core: 28
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 3219.533
CPU max MHz: 3500.000
CPU min MHz: 800.000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 43008K
NUMA node0 CPU(s): 0-13,56-69
NUMA node1 CPU(s): 14-27,70-83
NUMA node2 CPU(s): 28-41,84-97
NUMA node3 CPU(s): 42-55,98-111
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdmelpb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx flexcpu rcrdrandr lahf_lm abm 3nowprefetch cpuid_fault epb cat-13 invvpclmulqdq ssbd mba ibrs ibpb stibp ibrsenhanced tpr_shadow vmmi flexpriori ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaves비용 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local wbnoivnd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkgq Invalidate avx512vmbi umip pku ospke avx512_vmbi2 gfnia vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_lld

/proc/cpuinfo cache data

cache size : 43008 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69
node 0 size: 257634 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPEC CPU® 2017 Floating Point Rate Result

SPECrate®2017_fp_base = 387
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Cisco Systems
2.60GHz

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
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Platform Notes (Continued)

node 0 free: 257246 MB
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80
81 82 83
node 1 size: 258007 MB
node 1 free: 257376 MB
node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94
95 96 97
node 2 size: 258041 MB
node 2 free: 257761 MB
node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105
106 107 108 109 110 111
node 3 size: 258037 MB
node 3 free: 257742 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 1056482500 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECratenumber = 387
SPECratenumber = Not Run

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Platform Notes (Continued)

Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps
barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 May 21 23:47

SPECratenumber is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>14G</td>
<td>207G</td>
<td>7%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

| Vendor: | Cisco Systems Inc |
| Product: | UCSC-C220-M6S |
| Serial: | WZP24430ADF |

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

BIOS:
| BIOS Vendor: | Cisco Systems, Inc. |
| BIOS Version: | C220M6.4.2.1b.0.0512210554 |
| BIOS Date: | 05/12/2021 |
| BIOS Revision: | 5.22 |

(End of data from sysinfo program)

Compiler Version Notes

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

(Continued on next page)
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Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++             | 508.namd_r(base) 510.parest_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C          | 511.povray_r(base) 526.blender_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
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Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

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SPECrater\textsuperscript{2017}\textsubscript{fp\_peak} = Not Run

CPU\textsuperscript{2017} License: 9019
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Base Optimization Flags

C benchmarks:
\texttt{-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
\texttt{-mbranches-within-32B-boundaries -ljemalloc}
\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

C++ benchmarks:
\texttt{-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto}
\texttt{-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
\texttt{-mbranches-within-32B-boundaries -ljemalloc}
\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Fortran benchmarks:
\texttt{-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div}
\texttt{-qopt-prefetch -ffinite-math-only}
\texttt{-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4}
\texttt{-nostandard-realloc-lhs -align array32byte -auto}
\texttt{-mbranches-within-32B-boundaries -ljemalloc}
\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both Fortran and C:
\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo}
\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
\texttt{-qopt-multiple-gather-scatter-by-shuffles}
\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both C and C++:
\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
\texttt{-mbranches-within-32B-boundaries -ljemalloc}
\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using Fortran, C, and C++:
\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3}
\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
\texttt{-qopt-multiple-gather-scatter-by-shuffles}
\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.html
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6348, 2.60GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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