Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrater2017_fp_base = 454
SPECrater2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Hardware
CPU Name: Intel Xeon Platinum 8368Q
Max MHz: 3700
Nominal: 2600
Enabled: 76 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 57 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201113 for Linux;
Parallel: No
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
## Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

### SPECrate®2017_fp_base = 454
### SPECrate®2017_fp_peak = Not Run

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<td>Mar-2021</td>
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### Results Table

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</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

`LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"`

`MALLOC_CONF = "retain:true"`

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

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Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

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General Notes (Continued)

cpuinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on install Fri Jul 16 23:33:34 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
        2 "physical id"s (chips)
        152 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 38
siblings : 76

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on install Fri Jul 16 23:33:34 2021

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(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrate®2017_fp_base = 454
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35 36 37
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35 36 37

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 152
On-line CPU(s) list: 0-151
Thread(s) per core: 2
Core(s) per socket: 38
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
Stepping: 6
CPU MHz: 3300.000
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 58368K
NUMA node0 CPU(s): 0-37,76-113
NUMA node1 CPU(s): 38-75,114-151

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdempub rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
x86_movbe clflushopt clwb intel_pstate ssbd mba ibrs ibrd ibrs_Enhanced trp_shadow vni
flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt
avx512cd sha ni avx512bw avx512vl xsaves xsaveopt xsavevc xsavec xsaves cqm_llc
cqmm_mbm_total cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window
hwp_epp hwp_pkg_req avx512vbi umip pku ospke avx512vbmi2 gfnl vaes vpclmulqdq
avx512_vnni avx512_bitalg tme avx512 vpopedtq 1a57 rdpid md_clear pconfig flush_lid
arch_capabilities

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 58368 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus:  0  1  2  3  4  5  6  7  8  9  10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27
  28  29  30  31  32  33  34  35  36  37  38  39  40  41  42  43  44  45  46  47  48  49  50  51  52  53  54  55
  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75  76  77  78  79  80  81  82  83
  84  85  86  87  88  89  90  91  92  93  94  95  96  97  98  99  100  101  102  103  104  105  106  107  108
  109  110  111  112  113
  node 0 size: 1031767 MB
  node 0 free: 1029776 MB
  node 1 cpus: 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68
  69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101
  102 103 104 105 106 107 108 109 110 111 112 113
  node 1 size: 1032136 MB
  node 1 free: 1030781 MB
  node distances:
    node 0 1
    0: 10 20
    1: 20 10

From /proc/meminfo
  MemTotal: 2113437760 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)  

SPECrates

SPECrates

SPEC CPU®2017 Floating Point Rate Result

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Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrates

SPECrate®2017_fp_base = 454
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 16 19:45
SPEC is set to: /home/cpu2017
Filesystem     Type  Size  Used  Avail Use% Mounted on
/dev/sda2      btrfs  222G   15G  206G  7% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6SX
Serial: WZP24440K0A

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.1c.1.0701210708
BIOS Date: 07/01/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPEC CPU®2017 Floating Point Rate Result

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**Cisco Systems**
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

**SPECrate®2017_fp_base = 454**
**SPECrate®2017_fp_peak = Not Run**

---

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

---

**Compiler Version Notes (Continued)**

Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel (R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| C++             | 508.namd_r(base) 510.parest_r(base) |
---|---|
| Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel (R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  |
| C++, C          | 511.povray_r(base) 526.blender_r(base) |
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| Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel (R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  |
| C++, C, Fortran | 507.cactuBSSN_r(base) |
---|---|
| Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel (R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  |
| Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on Intel (R) 64,  
Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  |
| Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base) |
---|---|
| Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on Intel (R) 64,  
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(Continued on next page)
## Cisco Systems

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</table>

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### Compiler Version Notes (Continued)

- **Fortran, C**
  - 521.wrf_r(base)
  - 527.cam4_r(base)

---

### Base Compiler Invocation

- **C benchmarks**:
  - icx

- **C++ benchmarks**:
  - icpx

- **Fortran benchmarks**:
  - ifort

- **Benchmarks using both Fortran and C**:
  - ifort icx

- **Benchmarks using both C and C++**:
  - icpx icx

- **Benchmarks using Fortran, C, and C++**:
  - icpx icx ifort

---

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.ibm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)

549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -lipo
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,_muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,_muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

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<thead>
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<th>SPECrate®2017_fp_base =</th>
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<td>Not Run</td>
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CPU2017 License: 9019  
Test Date: Jul-2021  
Test Sponsor: Cisco Systems  
Hardware Availability: Apr-2021  
Tested by: Cisco Systems  
Software Availability: Mar-2021

### Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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