Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>165</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Copies</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
</tr>
<tr>
<td>508.namd_r</td>
</tr>
<tr>
<td>510.parest_r</td>
</tr>
<tr>
<td>511.povray_r</td>
</tr>
<tr>
<td>519.lbm_r</td>
</tr>
<tr>
<td>521.wrf_r</td>
</tr>
<tr>
<td>526.blender_r</td>
</tr>
<tr>
<td>527.cam4_r</td>
</tr>
<tr>
<td>538.imagick_r</td>
</tr>
<tr>
<td>544.nab_r</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
</tr>
<tr>
<td>554.roms_r</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base (165)</th>
</tr>
</thead>
<tbody>
<tr>
<td>206</td>
</tr>
<tr>
<td>105</td>
</tr>
<tr>
<td>159</td>
</tr>
<tr>
<td>142</td>
</tr>
<tr>
<td>163</td>
</tr>
<tr>
<td>141</td>
</tr>
<tr>
<td>149</td>
</tr>
<tr>
<td>159</td>
</tr>
<tr>
<td>373</td>
</tr>
<tr>
<td>243</td>
</tr>
<tr>
<td>148</td>
</tr>
<tr>
<td>78.4</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 5315Y
Max MHz: 3600
Nominal: 3200
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 12 MB I+D on chip per chip
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2933)
Storage: 1 x 240GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>peaks</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>503.bwaves_r</td>
<td>32</td>
<td>755</td>
<td>425</td>
<td>755</td>
<td>425</td>
<td>755</td>
<td>425</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>32</td>
<td>197</td>
<td>206</td>
<td>197</td>
<td>206</td>
<td>197</td>
<td>206</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>32</td>
<td>291</td>
<td>105</td>
<td>290</td>
<td>105</td>
<td>290</td>
<td>105</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>32</td>
<td>884</td>
<td>94.7</td>
<td>884</td>
<td>94.7</td>
<td>884</td>
<td>94.7</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>32</td>
<td>471</td>
<td>159</td>
<td>469</td>
<td>159</td>
<td>471</td>
<td>159</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>32</td>
<td>235</td>
<td>144</td>
<td>237</td>
<td>142</td>
<td>237</td>
<td>142</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>32</td>
<td>446</td>
<td>161</td>
<td>449</td>
<td>160</td>
<td>446</td>
<td>161</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>32</td>
<td>347</td>
<td>141</td>
<td>347</td>
<td>140</td>
<td>346</td>
<td>141</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>32</td>
<td>372</td>
<td>151</td>
<td>376</td>
<td>149</td>
<td>384</td>
<td>146</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>32</td>
<td>213</td>
<td>373</td>
<td>213</td>
<td>373</td>
<td>213</td>
<td>373</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>32</td>
<td>221</td>
<td>148</td>
<td>222</td>
<td>148</td>
<td>222</td>
<td>148</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>32</td>
<td>842</td>
<td>148</td>
<td>796</td>
<td>78.4</td>
<td>839</td>
<td>149</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>32</td>
<td>649</td>
<td>78.4</td>
<td>651</td>
<td>78.1</td>
<td>648</td>
<td>78.4</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 165**

**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The config file option 'submit' was used.
The numactl mechanism was used to bind copies to processors. The config file option 's' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

SPEC CPU®2017 Floating Point Rate Result

SPECrate®2017_fp_base = 165
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d
running on install Thu Sep 9 22:43:27 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5315Y CPU @ 3.20GHz
    2 "physical id"'s (chips)
    32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

CRC SPEC CPU2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECRate®2017_fp_base = 165
SPECRate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  Address sizes: 46 bits physical, 57 bits virtual
  CPU(s): 32
  On-line CPU(s) list: 0-31
  Thread(s) per core: 2
  Core(s) per socket: 8
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 106
  Model name: Intel(R) Xeon(R) Gold 5315Y CPU @ 3.20GHz
  Stepping: 6
  CPU MHz: 800.815
  CPU max MHz: 3600.0000
  CPU min MHz: 800.0000
  BogoMIPS: 6400.00
  Virtualization: VT-x
  L1d cache: 48K
  L1i cache: 32K
  L2 cache: 1280K
  L3 cache: 12288K
  NUMA node0 CPU(s): 0-7,16-23
  NUMA node1 CPU(s): 8-15,24-31
  Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdosp
class constant tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
  avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_1 invpcid_single ssbd
  mba ibpb stibp ibrs_enhanced tpr_shadow vni flexpriority ept vpid ept_ad
  fsbgbase tso_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f
  avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
  avx512bw avx512vl xsaveopt xsave cvtsid xsavec xsavec qcm llc qcm_occup llc qcm_mb_total
  qcm_mb_local wbnbio dtherm ida arat pln pts hwp hwp_act_window hwp_ese
  hwp_pke req avx512vmbi umip pku ospke avx512_vmbi qfni vaes vpclmulqdq avx512_vnni
  avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
  arch_capabilities
  /proc/cpuinfon cache data
  cache size : 12288 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

SPECrate®2017_fp_base = 165
SPECrate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Sep-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 1031780 MB
node 0 free: 1031193 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 1032150 MB
node 1 free: 1031695 MB
node distances:
node 0: 10 20
node 1: 20 10

From /proc/meminfo
MemTotal: 2113465672 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitation

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

SPECrated®2017_fp_base = 165
SPECrated®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 9 22:38

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>16G</td>
<td>206G</td>
<td>7%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6SX
Serial: WZP24440K0A

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.id.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)  

SPECrate®2017_fp_base = 165
SPECrate®2017_fp_peak = Not Run

CPU2017 License:  9019  
Test Sponsor:  Cisco Systems  
Test Date:  Sep-2021  
Hardware Availability:  Apr-2021  
Tested by:  Cisco Systems  
Software Availability:  Dec-2020

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------
C++, C  | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, 
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, 
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------
C++, C, Fortran  | 507.cactuBSSN_r(base)
------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, 
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, 
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on 
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------
Fortran  | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on 
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------
Fortran, C  | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on 
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, 
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

SPECraten®2017_fp_base = 165
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

**Base Compiler Invocation**

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)

SPECraten®2017_fp_base = 165
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbraches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbraches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbraches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbraches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbraches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Gold 5315Y, 3.20GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>165</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Sep-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

---

**SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.**

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-09-10 01:43:26-0400.  
Report generated on 2021-09-29 12:30:35 by CPU2017 PDF formatter v6442.  
Originally published on 2021-09-28.