Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6314U, 2.30GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed\textsuperscript{2017_int_base}</th>
<th>SPECspeed\textsuperscript{2017_int_peak}</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>32</td>
<td>7.98</td>
<td>10.7</td>
</tr>
<tr>
<td>gcc</td>
<td>32</td>
<td>5.79</td>
<td>6.95</td>
</tr>
<tr>
<td>mcf</td>
<td>32</td>
<td>11.0</td>
<td>17.4</td>
</tr>
<tr>
<td>omnetpp</td>
<td>32</td>
<td>4.75</td>
<td>5.79</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>32</td>
<td>13.1</td>
<td>19.7</td>
</tr>
<tr>
<td>x264</td>
<td>32</td>
<td>16.7</td>
<td>19.7</td>
</tr>
<tr>
<td>deepsjeng</td>
<td>32</td>
<td>4.75</td>
<td>4.75</td>
</tr>
<tr>
<td>leela</td>
<td>32</td>
<td>18.8</td>
<td>21.6</td>
</tr>
<tr>
<td>exchange2</td>
<td>32</td>
<td>11.0</td>
<td>11.0</td>
</tr>
<tr>
<td>xz</td>
<td>32</td>
<td>5.79</td>
<td>5.79</td>
</tr>
</tbody>
</table>

**Hardware**
- CPU Name: Intel Xeon Gold 6314U
- Max MHz: 3400
- Nominal: 2300
- Enabled: 32 cores, 1 chip
- Orderable: 1 Chips
- Cache L1: 32 KB I + 48 KB D on chip per core
- L2: 1.25 MB I+D on chip per core
- L3: 48 MB I+D on chip per chip
- Other: None
- Memory: 512 GB (16 x 32 GB 2Rx4 PC4-3200V-R)
- Storage: 1 x 960 GB M.2 SSD SATA
- Other: None

**Software**
- OS: SUSE Linux Enterprise Server 15 SP2 (x86_64) 5.3.18-22-default
- Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- Parallel: Yes
- Firmware: Version 4.2.1d released Jul-2021
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: jemalloc memory allocator V5.0.1
- Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6314U, 2.30GHz)
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**

Cisco UCS C220 M6 (Intel Xeon Gold 6314U, 2.30GHz)  

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

**General Notes (Continued)**


**Platform Notes**

BIOS Settings:
- Intel Hyper-Threading Technology set to Disabled
- DCU Streamer Prefetch set to Disabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d  
running on localhost Mon Oct 11 02:49:41 2021

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6314U CPU @ 2.30GHz
  1 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
```

From lscpu from util-linux 2.33.1:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
Address sizes:         46 bits physical, 57 bits virtual
CPU(s):                32
On-line CPU(s) list:   0-31
Thread(s) per core:    1
Core(s) per socket:    32
Socket(s):             1
NUMA node(s):          1
Vendor ID:             GenuineIntel
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6314U, 2.30GHz)
## Platform Notes (Continued)

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version* 

os-release: 
NAME="SLES" 
VERSION="15-SP2" 
VERSION_ID="15.2" 
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2" 
ID="sles" 
ID_LIKE="suse" 
ANSI_COLOR="0;32" 
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a: 
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: userscopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Oct 11 02:37
SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>31G</td>
<td>191G</td>
<td>14%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP24430ADF

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6314U, 2.30GHz)

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Platform Notes (Continued)

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
16x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200
16x NO DIMM NO DIMM

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C     | 600.perlbench_s(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C     | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C     | 600.perlbench_s(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
C     | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
(Continued on next page)
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**Tested by:** Cisco Systems

**Compiler Version Notes (Continued)**

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++
---
620.omnetpp_s (base, peak) 623.xalancbmk_s (base, peak)
631.deepsjeng_s (base, peak) 641.leela_s (base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran
---
648.exchange2_s (base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

**Base Portability Flags**

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64

(Continued on next page)
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SPEC®2017_int_base = 11.5
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Base Portability Flags (Continued)

641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

600.perlbench_s: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
# SPEC CPU®2017 Integer Speed Result

## Cisco Systems

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### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

#### C benchmarks:

- **600.perlbench_s**: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)  
  -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=4 -fno-strict-overflow  
  -mbranches-within-32B-boundaries  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **602.gcc_s**: `-m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)  
  -fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto  
  -Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4  
  -mbranches-within-32B-boundaries  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **605.mcf_s**: basepeak = yes

- **625.x264_s**: `-DSPEC_OPENMP -fipenmp -std=c11 -m64 -Wl,-z,muldefs  
  -xCORE-AVX512 -flto -O3 -ffast-math  
  -qopt-mem-layout-trans=4 -fno-alias  
  -mbranches-within-32B-boundaries  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **657.xz_s**: basepeak = yes

#### C++ benchmarks:

- **620.omnetpp_s**: basepeak = yes

- **623.xalancbmk_s**: basepeak = yes

- **631.deepsjeng_s**: basepeak = yes

- **641.leela_s**: basepeak = yes

#### Fortran benchmarks:

- **648.exchange2_s**: basepeak = yes
## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

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The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: