Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 5318N, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 169</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = Not Run</td>
</tr>
</tbody>
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**Threads**

- 603.bwaves_s 48
- 607.cactuBSSN_s 48
- 619.lbm_s 48
- 621.wrf_s 48
- 627.cam4_s 48
- 628.pop2_s 48
- 638.imagick_s 48
- 644.nab_s 48
- 649.fotonik3d_s 48
- 654.roms_s 48

**Software**

- OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- Compiler: Fortran: Version 2021.4.0 of Intel Fortran Compiler
- C/C++: Version 2021.4.0 of Intel C/C++ Compiler Classic Build 20210910 for Linux;
- Parallel: Yes
- Firmware: Version 5.0.1d released Aug-2021
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other: jemalloc memory allocator V5.0.1
- Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

**Hardware**

- CPU Name: Intel Xeon Gold 5318N
- Max MHz: 3400
- Nominal: 2100
- Enabled: 48 cores, 2 chips
- Orderable: 1.2 Chips
- Cache L1: 32 KB I + 48 KB D on chip per core
- L2: 1.25 MB I+D on chip per core
- L3: 36 MB I+D on chip per chip
- Other: None
- Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
- Storage: 1 x 240 GB M.2 SSD SATA
- Other: None

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Page 1 Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/
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SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 169
SPECspeed®2017_fp_peak = Not Run

Results Table

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<th>Ratio</th>
<th>Seconds</th>
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<td>78.7</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
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Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Intel Hyper-Threading Technology set to Disable
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on perf-blade5 Wed Dec 8 10:32:13 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5318N CPU @ 2.10GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318N CPU @ 2.10GHz
Stepping: 6
CPU MHz: 1969.485

(Continued on next page)
**Cisco Systems**

Cisco UCS X210c M6 (Intel Xeon Gold 5318N, 2.10GHz)

**SPECspeed®2017_fp_base** = 169

**SPECspeed®2017_fp_peak** = Not Run

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**Platform Notes (Continued)**

- CPU max MHz: 3400.0000
- CPU min MHz: 800.0000
- BogoMIPS: 4200.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 36864K
- NUMA node0 CPU(s): 0-23
- NUMA node1 CPU(s): 24-47
- Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invol羲e_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bml hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaveas cqm_llc cqm_occup_llc cqm_mmb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwlp act_window hwlp epp hwlp pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lld arch_capabilities

/proc/cpuinfo cache data
  cache size : 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  node 0 size: 1031779 MB
  node 0 free: 1027786 MB
  node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 1 size: 1032148 MB
  node 1 free: 1031306 MB
  node distances:
    node 0 1
    0: 10 20
    1: 20 10

From /proc/meminfo
  MemTotal: 2113462352 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

(Continued on next page)
## Platform Notes (Continued)

```bash
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

```bash
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"
```

```bash
uname -a:
  Linux perf-blade5 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
  x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-12207** (iTLB Multihit): Not affected
- **CVE-2018-3620** (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- **CVE-2017-5754** (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2018-3639** (Speculative Store Bypass): Mitigation: usercopy/swaps barriers and __user pointer sanitization
- **CVE-2017-5753** (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2017-5715** (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543** (Special Register Buffer Data Sampling): Not affected
- **CVE-2019-11135** (TSX Asynchronous Abort): Not affected

run-level 3 Dec 8 07:51

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sdb2</td>
<td>btrfs</td>
<td>224G</td>
<td>55G</td>
<td>169G</td>
<td>25%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

| Vendor:            | Cisco Systems Inc
| Product:           | UCSX-210C-M6
| Serial:            | FCH250671LG

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you

(Continued on next page)
## Platform Notes (Continued)

interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

- 32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:

- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: X210M6.5.0.1d.0.0816211754
- BIOS Date: 08/16/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

### Compiler Version Notes

<table>
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<tr>
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<th>638.imagick_s(base)</th>
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<th>654.roms_s(base)</th>
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SPECspeed®2017_fp_base = 169
SPECspeed®2017_fp_peak = Not Run

==-= Compiler Version Notes (Continued) ==-=

Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==-= Base Compiler Invocation ==-=

C benchmarks:
icc
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icc
Benchmarks using Fortran, C, and C++:
icpc icc ifort

==-= Base Portability Flags ==-=

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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| Tested by: | Cisco Systems |
| Hardware Availability: | Sep-2021 |
| Software Availability: | Sep-2021 |

**Base Optimization Flags**

C benchmarks:
- `-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
- `-mbranches-within-32B-boundaries`

Fortran benchmarks:
- `-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-nostandard-realloc-lhs -mbranches-within-32B-boundaries`
- `-L/home/cpu2017/je5.0.1-64 -ljemalloc`

Benchmarks using both Fortran and C:
- `-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs`
- `-L/home/cpu2017/je5.0.1-64 -ljemalloc`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs`
- `-L/home/cpu2017/je5.0.1-64 -ljemalloc`

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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