Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

SPECompG_peak2012 = Not Run
SPECompG_base2012 = 40.2

OMP2012 license: 9019
Test sponsor: Cisco Systems
Test date: Oct-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Sep-2017

| Threads | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 170 | 180 | 190 | 195 |
|---------|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 350.md  | 224 | 38.8 |
| 351.bwaves | 224 | 33.1 |
| 352.nab  | 224 | 51.7 |
| 357.bt331 | 224 | 35.1 |
| 358.botsalgn | 224 | 23.3 |
| 359.botsspar | 224 | 26.2 |
| 360.ilbdc | 224 | 31.5 |
| 362.fma3d | 224 | 29.9 |
| 363.swim | 224 | 45.6 |
| 367.imagick | 224 | 26.2 |
| 370.mgrid331 | 224 | 32.6 |
| 371.applu331 | 224 | 82.7 |
| 372.smithwa | 224 | 35.3 |
| 376.kdtree | 224 | 35.3 |

SPECompG_base2012 = 40.2

---

**Hardware**

- CPU Name: Intel Xeon Platinum 8180
- CPU Characteristics: Intel Turbo Boost Technology up to 3.80 GHz
- CPU MHz: 2500
- CPU MHz Maximum: 3800
- FPU: Integrated
- CPU(s) enabled: 112 cores, 4 chips, 28 cores/chip, 2 threads/core
- CPU(s) orderable: 2,4 Chips
- Primary Cache: 32 KB I + 32 KB D on chip per core
- Secondary Cache: 1 MB I+D on chip per core
- L3 Cache: 38.5 MB I+D on chip per chip
- Other Cache: None
- Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- Disk Subsystem: 1 X 480 GB SSD SAS
- Other Hardware: None
- Base Threads Run: 224
- Minimum Peak Threads: --

---

**Software**

- Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64)
- Compiler: C/C++/Fortran; Version 18.0.0.128 of Intel Composer for Linux Build 20170811
- Auto Parallel: No
- File System: xfs
- System State: Run Level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other Software: None
Cisco Systems

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SPECompG_peak2012 = Not Run
SPECompG_base2012 = 40.2

OMP2012 license: #9019
Test sponsor: Cisco Systems
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Maximum Peak Threads: --

Results Table

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<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Platform Notes

Sysinfo program /home/omp2012/Docs/sysinfo
$Rev: 395 $ $Date:: 2012-07-25 #$ 8f8c0fe9e19c658963a1e67685e50647
running on C480-SLES12 Fri Oct 6 16:58:05 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/omp2012/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
  4 "physical id"s (chips)
  224 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
  25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
  25 26 27 28 29 30
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
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Cisco Systems
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</table>

Platform Notes (Continued)

- physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
- cache size: 39424 KB

From /proc/meminfo
- MemTotal: 790981324 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version* SuSE-release:
- NAME="SLES"
- VERSION="12-SP2"
- VERSION_ID="12.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
- ID="sles"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:12:sp2"

unname -a:
  (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Oct 5 13:19

SPEC is set to: /home/omp2012
- /dev/sda3  xfs  404G  79G  326G  20% /home

Additional information from dmidecode:
- BIOS Cisco Systems, Inc. C480M5.3.1.0.272.0613172154 06/13/2017
- Memory:
  - 48x 16 GB
  - 48x 0xCE00 M393A2G40EB2-CTD 16 GB 2666 MHz 2 rank

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

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OMP2012 license: 9019  
Test sponsor: Cisco Systems  
Tested by: Cisco Systems

General Notes

BIOS settings notes:
- Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/transparent_hugepage/enabled

BIOS settings notes:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- Sub Numa Clustering (SNC) set to Disabled
- IMC Interleaving set to Auto

General OMP Library Settings
- ENV_KMP_LIBRARY=turnaround
- ENV_OMP_SCHEDULE=static
- ENV_KMP_BLOCKTIME=200
- ENV_KMP_STACKSIZE=16G
- ENV_OMP_DYNAMIC=FALSE
- ENV_OMP_NESTED=FALSE

General base OMP Library Settings
- ENV_KMP_AFFINITY=compact,1

Base Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

Base Portability Flags

350.md: -FR
357.bt331: -mcmodel=medium
363.swim: -mcmodel=medium
367.imagick: -std=c99

Base Optimization Flags

C benchmarks:
- -O3 -qopenmp -ipo -xHost -ansi-alias

Continued on next page
## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

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| Test sponsor:   | Cisco Systems |
| Tested by:      | Cisco Systems |
| Test date:      | Oct-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Sep-2017 |

### Base Optimization Flags (Continued)

C++ benchmarks:
- `-O3` `-qopenmp` `-ipo` `-xHost` `-ansi-alias`

Fortran benchmarks:
- `-O3` `-qopenmp` `-ipo` `-xHost` `-align array64byte`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/omp2012/flags/Intel-ic18.0-linux64.html](http://www.spec.org/omp2012/flags/Intel-ic18.0-linux64.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/omp2012/flags/Intel-ic18.0-linux64.xml](http://www.spec.org/omp2012/flags/Intel-ic18.0-linux64.xml)

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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