Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280, 2.70 GHz)

SPECompG_peak2012 = Not Run
SPECompG_base2012 = 44.9

| Threads | 0.00 | 10.00 | 20.00 | 30.00 | 40.00 | 50.00 | 60.00 | 70.00 | 80.00 | 90.00 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 170 | 180 | 190 | 200 | 210 | 220 | 230 | 240 | 250 | 260 | 270 | 280 | 290 | 300 | 310 | 320 | 330 | 340 | 350 | 360 | 370 | 380 | 390 | 400 | 410 | 420 | 430 | 440 | 450 | 460 | 470 | 480 | 490 | 500 | 510 | 520 | 530 | 540 | 550 | 560 | 570 | 580 | 590 | 600 | 610 | 620 | 630 | 640 | 650 | 660 | 670 | 680 | 690 | 700 | 710 | 720 | 730 | 740 | 750 | 760 | 770 | 780 | 790 | 800 | 810 | 820 | 830 | 840 | 850 | 860 | 870 | 880 | 890 | 900 | 910 | 920 | 930 | 940 | 950 | 960 | 970 | 980 | 990 | 1000 | 1010 | 1020 | 1030 | 1040 | 1050 | 1060 | 1070 | 1080 | 1090 | 1100 | 1110 | 1120 | 1130 | 1140 | 1150 | 1160 | 1170 | 1180 | 1190 | 1200 | 1210 | 1220 | 1230 | 1240 | 1250 | 1260 | 1270 | 1280 | 1290 | 1300 | 1310 | 1320 | 1330 | 1340 | 1350 | 1360 | 1370 | 1380 | 1390 | 1400 | 1410 | 1420 | 1430 | 1440 | 1450 | 1460 | 1470 | 1480 | 1490 | 1500 | 1510 | 1520 | 1530 | 1540 | 1550 | 1560 | 1570 | 1580 | 1590 | 1600 | 1610 | 1620 | 1630 | 1640 | 1650 | 1660 | 1670 | 1680 | 1690 | 1700 | 1710 | 1720 | 1730 | 1740 | 1750 | 1760 | 1770 | 1780 | 1790 | 1800 | 1810 | 1820 | 1830 | 1840 | 1850 | 1860 | 1870 | 1880 | 1890 | 1900 | 1910 | 1920 | 1930 | 1940 | 1950 | 1960 | 1970 | 1980 | 1990 | 2000 | 2010 | 2020 | 2030 | 2040 | 2050 | 2060 | 2070 | 2080 | 2090 | 2100 | 2110 | 2120 | 2130 | 2140 | 2150 | 2160 | 2170 | 2180 | 2190 | 2200 | 2210 | 2220 | 2230 | 2240 | 2250 | 2260 | 2270 | 2280 | 2290 | 2300 | 2310 | 2320 | 2330 | 2340 | 2350 | 2360 | 2370 | 2380 | 2390 | 2400 | 2410 | 2420 | 2430 | 2440 | 2450 |

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SPECompG_base2012 = 44.9

Hardware

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<td>Intel Xeon Platinum 8280</td>
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<tr>
<td>CPU Characteristics</td>
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</tr>
<tr>
<td>CPU MHz</td>
<td>2700</td>
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<td>CPU MHz Maximum</td>
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<tr>
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<td>Integrated</td>
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<td>CPU(s) orderable</td>
<td>2,4 Chips</td>
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<tr>
<td>Primary Cache</td>
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<td>Secondary Cache</td>
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<td>Memory</td>
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<td>Minimum Peak Threads</td>
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Software

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<td>Compiler</td>
<td>C/C++/Fortran; Version 19.0.1.144 of Intel Composer for Linux Build 20181018</td>
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<tr>
<td>File System</td>
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<td>System State</td>
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<td>Base Pointers</td>
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<td>Peak Pointers</td>
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Continued on next page
## SPEC OMPG2012 Result

**Cisco Systems**  
Cisco UCS C480 M5 (Intel Xeon Platinum 8280, 2.70 GHz)  

**SPECompG_peak2012 = Not Run**  
**SPECompG_base2012 = 44.9**

**OMP2012 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**Maximum Peak Threads:** --  
**Test date:** Mar-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** Mar-2019

### Results Table

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<td><strong>34.6</strong></td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Platform Notes

Sysinfo program /home/OMP2012/Docs/sysinfo  
Revision 563 of 2016-06-10 (097295389cfe6073d8c3b03fa376740a5)  
running on linux-mz3p Fri Mar 8 02:30:13 2019

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: http://www.spec.org/omp2012/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
4 "physical id"s (chips)
224 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30
```

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280, 2.70 GHz)

SPECompG_peak2012 = Not Run
SPECompG_base2012 = 44.9

Platform Notes (Continued)

physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30

From /proc/meminfo
MemTotal: 1583861556 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME=SLES
VERSION=15
VERSION_ID=15
PRETTY_NAME=SUSE Linux Enterprise Server 15
ID=sles
ID_LIKE=suse
ANSI_COLOR=0;32
CPE_NAME=cpe:/o:suse:sles:15

uname -a:
Linux linux-mz3p 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018
(cd0437b) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Mar 7 20:39

SPEC is set to: /home/OMP2012

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 549G 36G 513G 7% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.4.0.3.17.0213191844 02/13/2019
Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933 MT/s, configured at 2934 MT/s

(End of data from sysinfo program)

General Notes
========================================================================
BIOS settings notes:
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
BIOS settings notes:
Intel Turbo Boost Technology (Turbo) : Enabled
CPU performance set to Enterprise

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280, 2.70 GHz)

SPECompG_peak2012 = Not Run
SPECompG_base2012 = 44.9

OMP2012 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
General OMP Library Settings
ENV_KMP_LIBRARY=turnaround
ENV_OMP_SCHEDULE=static
ENV_KMP_BLOCKTIME=200
ENV_KMP_STACKSIZE=702M
ENV_OMP_DYNAMIC=FALSE
ENV_OMP_NESTED=FALSE

General base OMP Library Settings
ENV_KMP_AFFINITY=compact,1

Spectre and Meltdown
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Base Compiler Invocation

C benchmarks:
  icc
C++ benchmarks:
  icpc
Fortran benchmarks:
  ifort

Base Portability Flags

350.md: -FR
357.bt331: -mcmode=medium
363.swim: -mcmode=medium
367.imagick: -std=c99

Base Optimization Flags

C benchmarks:
  -O3 -qopenmp -ipo -xCORE-AVX512 -ansi-alias

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280, 2.70 GHz)

<table>
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<th>SPEC OMPG2012 Result</th>
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**Test date:** Mar-2019
**Test sponsor:** Cisco Systems
**Tested by:** Cisco Systems

**Test date:** Mar-2019
**Hardware Availability:** Apr-2019
**Software Availability:** Mar-2019

**OMP2012 license:** 9019

---

**Base Optimization Flags (Continued)**

**C++ benchmarks:**
- -O3 -qopenmp -ipo -xCORE-AVX512 -ansi-alias

**Fortran benchmarks:**
- -O3 -qopenmp -ipo -xCORE-AVX512 -align array64byte

---

The flags files that were used to format this result can be browsed at:
http://www.spec.org/omp2012/flags/Intel-ic19.0-linux64.html
http://www.spec.org/omp2012/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/omp2012/flags/Intel-ic19.0-linux64.xml
http://www.spec.org/omp2012/flags/Cisco-Platform-Settings-V1.2-revH.xml

---

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC OMP2012 v1.1.
Originally published on 30 April 2019.