CINT2000 Result

Hewlett-Packard Company
hp AlphaServer GS80 68/1224

SPECint_rate2000 = NC

SPECint_rate_base2000 = NC

SPEC license #: 2 | Tested by: HPQ - NH | Test date: Jul-2002 | Hardware Avail: Aug-2002 | Software Avail: Nov-2001

SPEC has determined that this result was not in compliance with the SPEC CPU2000 run and reporting rules. Specifically, the submitter has reported that the 3 month availability requirement in the SPEC CPU2000 run rules will not be met due to a change in availablility date for the operating system.

Benchmark	Base Copies	Base Runtime	Base Ratio	Copies	Runtime	Ratio
164.gzip	1	NC	NC	1	NC	NC
175.vpr	1	NC	NC	1	NC	NC
176.gcc	1	NC	NC	1	NC	NC
181.mcf	1	NC	NC	1	NC	NC
186.crafty	1	NC	NC	1	NC	NC
197.parser	1	NC	NC	1	NC	NC
252.eon	1	NC	NC	1	NC	NC
253.perlbmk	1	NC	NC	1	NC	NC
254.gap	1	NC	NC	1	NC	NC
255.vortex	1	NC	NC	1	NC	NC
256.bzip2	1	NC	NC	1	NC	NC
300.twolf	1	NC	NC	1	NC	NC

Hardware

CPU:	Alpha 21264C
CPU MHz:	1224
FPU:	Integrated
CPU(s) enabled:	1 core, 1 chip, 1 core/chip
CPU(s) orderable:	1 to 8
Parallel:	No
Primary Cache:	64KB(I)+64KB(D) on chip
Secondary Cache:	16MB off chip per CPU
L3 Cache:	None
Other Cache:	None
Memory:	16GB
Disk Subsystem:	9GB Hard Drive
Other Hardware:	None

Software

Operating System:	Tru64 UNIX V5.1B
Compiler:	Compaq C V6.4-215-46B7O Program Analysis Tools V2.0 Spike V5.2 DTK (1.471.2.2 46B5P) Compaq C++ V6.3-010-46B2F
File System:	ufs
System State:	Multi-user

Notes/Tuning Information

```
Baseline C  : cc  -arch ev6 -fast +CFB ONESTEP
        C++: cxx -arch ev6 -O2        ONESTEP

Peak:
  All but 252.eon: cc -g3 -arch ev6 ONESTEP
     164.gzip: -fast -O4 -non_shared +CFB
      175.vpr: -fast -O4 -assume restricted_pointers +CFB
      176.gcc: -fast -O4 -xtaso_short -all -ldensemalloc -none
               +CFB +IFB
```

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Notes/Tuning Information (Continued)

```
      181.mcf: -fast -xtaso_short +CFB +IFB +PFB
   186.crafty: same as base
   197.parser: -fast -O4 -xtaso_short -non_shared +CFB
      252.eon: cxx -arch ev6 -O2 -all -ldensemalloc -none
  253.perlbmk: -fast -non_shared +CFB +IFB
      254.gap: -fast -O4 -non_shared +CFB +IFB +PFB
   255.vortex: -fast -non_shared +CFB +IFB
    256.bzip2: -fast -O4 -non_shared +CFB
    300.twolf: -fast -O4
               -ldensemalloc -non_shared +CFB +IFB

Most benchmarks are built using one or more types of
profile-driven feedback.  The types used are designated
by abbreviations in the notes:

+CFB: Code generation is optimized by the compiler, using
      feedback from a training run.  These commands are
      done before the first compile (in phase "fdo_pre0"):

           mkdir /tmp/pp
           rm -f /tmp/pp/${baseexe}*

      and these flags are added to the first and second compiles:

           PASS1_CFLAGS = -prof_gen_noopt -prof_dir /tmp/pp
           PASS2_CFLAGS = -prof_use       -prof_dir /tmp/pp

    (Peak builds use /tmp/pp above; base builds use /tmp/pb.)

+IFB: Icache usage is improved by the post-link-time optimizer
      Spike, using feedback from a training run.  These commands
      are used (in phase "fdo_postN"):

           mv ${baseexe} oldexe
           spike oldexe -feedback oldexe -o ${baseexe}

+PFB: Prefetches are improved by the post-link-time optimizer
      Spike, using feedback from a training run.  These
      commands are used (in phase "fdo_post_makeN"):

           rm -f *Counts*
           mv ${baseexe} oldexe
           pixie -stats dstride oldexe 1>pixie.out 2>pixie.err
           mv oldexe.pixie ${baseexe}
```

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Notes/Tuning Information (Continued)

```
        A training run is carried out (in phase "fdo_runN"), and
        then this command (in phase "fdo_postN"):

             spike oldexe -fb oldexe -stride_prefetch -o ${baseexe}

    When Spike is used for both Icache and Prefetch improvements,
    only one spike command is actually issued, with the Icache
    options followed by the Prefetch options.

    Portability: gcc: -Dalloca=__builtin_alloca; crafty: -DALPHA
    perlbmk: -DSPEC_CPU2000_DUNIX; vortex: -DSPEC_CPU2000_LP64
    gap: -DSYS_HAS_CALLOC_PROTO -DSYS_IS_BSD -DSYS_HAS_IOCTL_PROTO
         -DSPEC_CPU2000_LP64

    vm:
            vm_bigpg_enabled = 1
            vm_bigpg_thresh = 16
            vm_swap_eager = 0

    proc:
            max_per_proc_address_space = 0x40000000000
            max_per_proc_data_size = 0x40000000000
            max_per_proc_stack_size = 0x40000000000
            max_proc_per_user = 2048
            max_threads_per_user = 0
            maxusers = 16384
            per_proc_address_space = 0x40000000000
            per_proc_data_size = 0x40000000000
            per_proc_stack_size = 0x40000000000

    System is single QBB (4-cpu) with only 1 cpu enabled at console


  Submitted_by: "Beer, Chris" <Chris.Beer@hp.com>
  Submitted: Thu Aug  1 16:15:29 2002
  Submission: cpu2000-20020801-01535.sub
```