



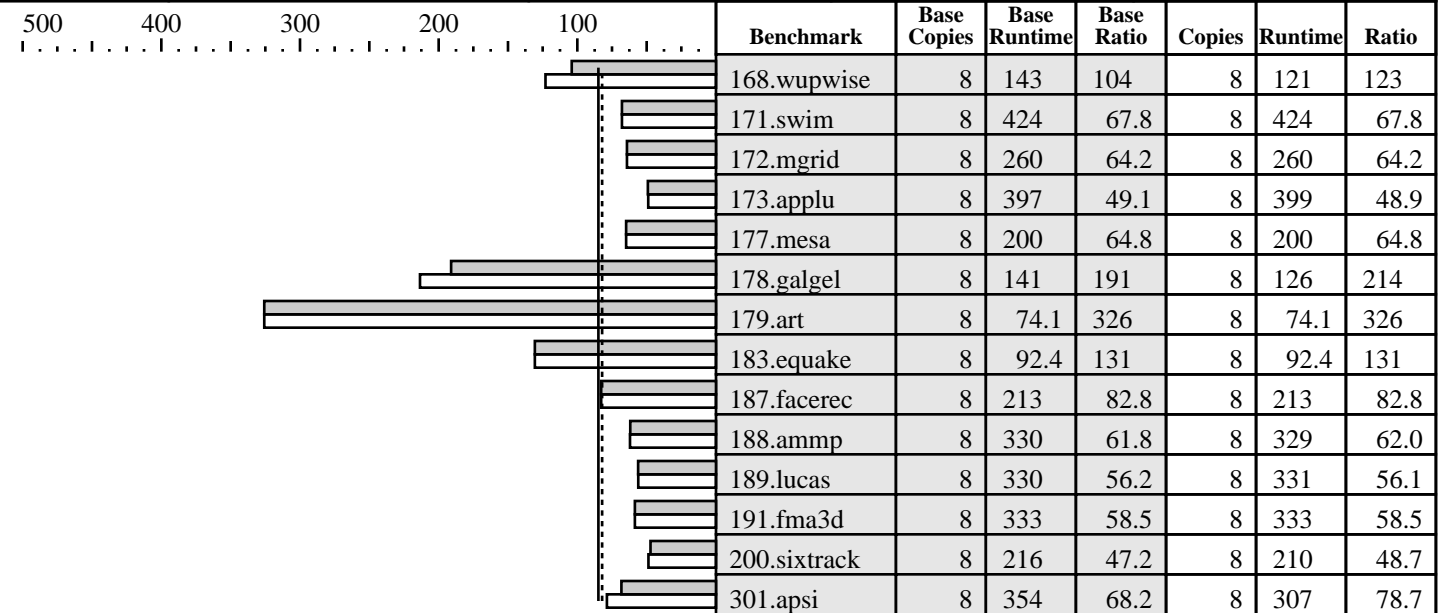
CFP2000 Result

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IBM Corporation
IBM eServer p5 550 (1650 MHz, 4 CPU)

SPECfp_rate2000 = 84.8
SPECfp_rate_base2000 = 82.1

SPEC license #: 11 | Tested by: IBM | Test date: Jun-2004 | Hardware Avail: Aug-2004 | Software Avail: Oct-2004



Hardware

CPU: POWER5
 CPU MHz: 1650
 FPU: Integrated
 CPU(s) enabled: 4 cores, 2 chips, 2 cores/chip (SMT on)
 CPU(s) orderable: 2,4
 Parallel: No
 Primary Cache: 64KBI+32KBD (on chip)/core
 Secondary Cache: 1920KB unified (on chip)/chip
 L3 Cache: 36MB unified (off chip)/DCM, 2 DCM/SUT
 Other Cache: none
 Memory: 16x4 GB
 Disk Subsystem: 1x36GB SCSI, 15K RPM
 Other Hardware:

Software

Operating System: AIX 5L V5.3
 Compiler: XL C/C++ Enterprise Edition Version 7.0 for AIX
 XL Fortran Enterprise Edition V9.1 for AIX
 Other Software: IBM Engineering and Scientific Subroutine Library for AIX, Version 4 Release 2
 File System: AIX/JFS2
 System State: Multi-User

Notes/Tuning Information

Portability Flags

-qfixed used in: 168.wupwise, 171.swim, 172.mgrid, 173.applu,
 178.galgel, 200.sixtrack, 301.apsi
 -qsuffix=f=f90 used in: 178.galgel, 187.facerec, 189.lucas, 191.fma3d

Base Optimization Flags:

C: -qpdf1/pdf2 -O5 -blpdata -qalign=natural
 Fortran: -qpdf1/pdf2 -O5 -blpdata -lmass

Peak Optimization Flags

168.wupwise: -O5 -qarch=pwr3 -qtune=pwr3 -blpdata -lmass
 F77 = xlf
 171.swim: basepeak = 1
 172.mgrid: basepeak = 1
 173.applu: -O5 -blpdata -lmass



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Notes/Tuning Information (Continued)

```

177.mesa:      basepeak = 1
178.galgel:    -O5 -blpdata -qessl -lessl
179.art:       basepeak = 1
183.earthquake: basepeak = 1
187.facerec:   basepeak = 1
188.ammp:      -qpdf1/pdf2
               -O5 -blpdata -qalign=natural -D_ILS_MACROS
189.lucas:     -O5 -blpdata -lmass
191.fma3d:     basepeak = 1
200.sixtrack:  fdpr -quiet -R3
               -O3 -qhot -qarch=pwr5 -qtune=pwr5 -qfdpr
301.apsi:      -O5 -lmass -qessl -lessl -blpdata -qsave

```

SMT: Acronym for "Simultaneous Multi-Threading". A processor technology that allows the simultaneous execution of multiple thread contexts within a single processor core. (Enabled by default)

DCM: Acronym for "Dual-Chip Module" (one dual-core processor chip + one L3-cache chip)

SUT: Acronym for "System Under Test"

ulimits set to unlimited.

Large page mode and memory affinity were set as follows:

```

vmo -r -o lpgg_regions=400 -o lpgg_size=16777216 -o memory_affinity=1
chuser capabilities=CAP_BYPASS_RAC_VMM,CAP_PROPAGATE $USER
reboot -q
export MEMORY_AFFINITY=MCM

```