SPEC® CFP2006 Result

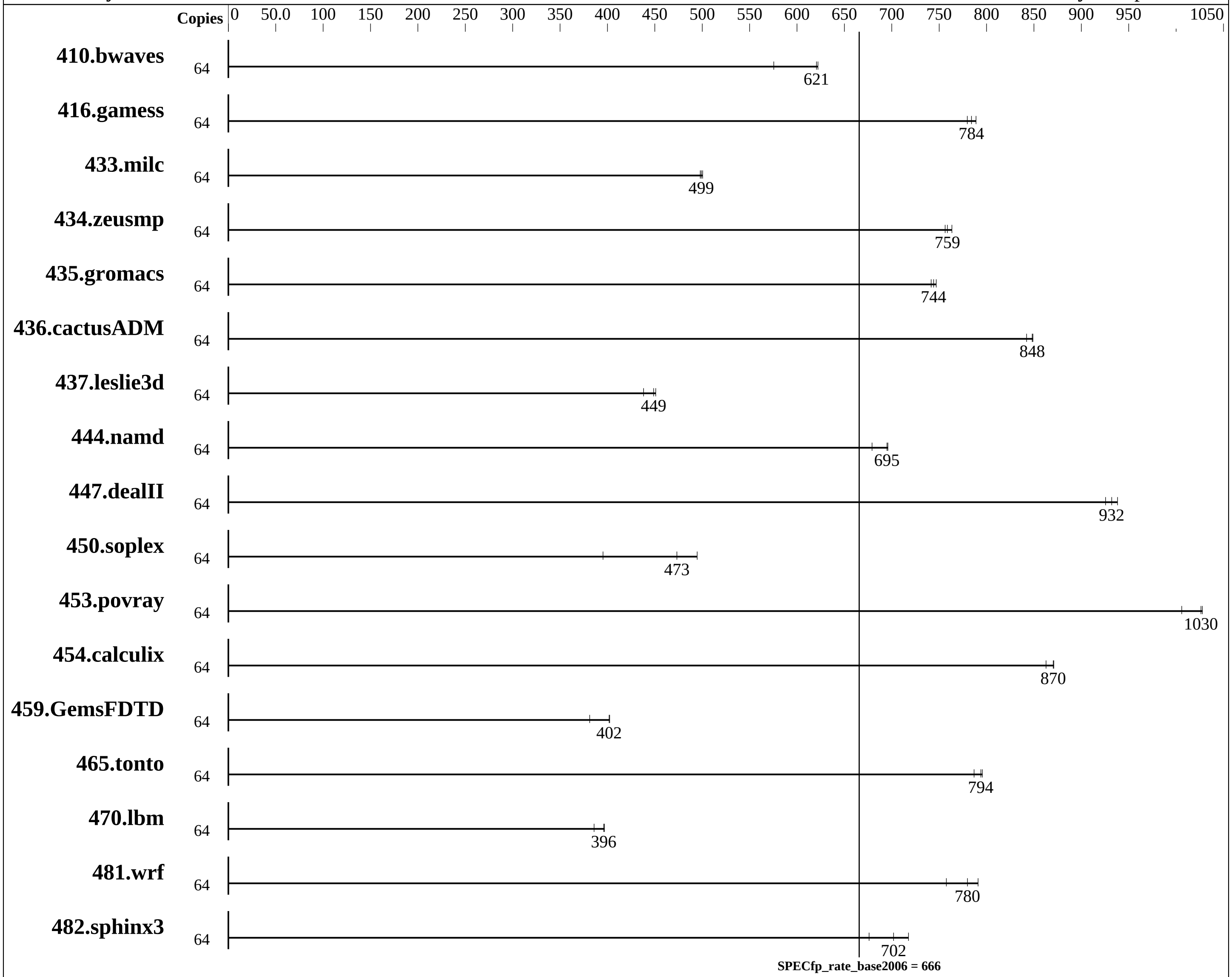
ScaleMP

vSMP Foundation (Intel Xeon X5570, see notes)

SPECfp®_rate2006 = Not Run

SPECfp_rate_base2006 = 666

CPU2006 license:	2929	**Test date:**	Apr-2009
Test sponsor:	ScaleMP	**Hardware Availability:**	Apr-2009
Tested by:	ScaleMP	**Software Availability:**	Apr-2009



Hardware

CPU Name:	Intel Xeon X5570
CPU Characteristics:	Intel Turbo Boost Technology disabled
CPU MHz:	2933
FPU:	Integrated
CPU(s) enabled:	32 cores, 8 chips, 4 cores/chip, 2 threads/core
CPU(s) orderable:	4,6,8,10,12,14,16,18,20,22,24,26,28,30,32 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core

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Software

Operating System:	Red Hat Enterprise Linux Server release 5.1 (Tikanga) Kernel: 2.6.21.7-13.vSMP
Compiler:	Intel C Compiler for applications running on Intel 64, Version 11.0.074 Intel Fortran Compiler for applications running on Intel 64, Version 11.0.074
Auto Parallel:	No
File System:	xfs

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L3 Cache:	8 MB I+D on chip per chip	System State:	Multi-user, run level 3
Other Cache:	20 GB I+D off chip per entire system (see notes)	Base Pointers:	64-bit
Memory:	192 GB (4 x 12 x 4 GB DDR3-1333R, ECC, CL9)	Peak Pointers:	Not Applicable
Disk Subsystem:	4 x 1 x 500 GB SATA, 7200 RPM	Other Software:	ScaleMP vSMP Foundation 2.0.44.0
Other Hardware:	InfiniBand		

Results Table

	Base							Peak						
Benchmark	**Copies**	**Seconds**	**Ratio**	**Seconds**	**Ratio**	**Seconds**	**Ratio**	**Copies**	**Seconds**	**Ratio**	**Seconds**	**Ratio**	**Seconds**	**Ratio**
410.bwaves	64	1511	575	**1402**	**621**	1398	622							
416.gamess	64	1607	780	1588	789	**1598**	**784**							
433.milc	64	**1177**	**499**	1180	498	1174	500							
434.zeusmp	64	770	756	763	763	**768**	**759**							
435.gromacs	64	616	742	**614**	**744**	612	747							
436.cactusADM	64	**902**	**848**	908	842	901	849							
437.leslie3d	64	1373	438	**1341**	**449**	1334	451							
444.namd	64	756	679	**739**	**695**	738	696							
447.dealII	64	791	926	780	938	**786**	**932**							
450.soplex	64	1350	395	**1128**	**473**	1079	495							
453.povray	64	338	1010	**332**	**1030**	331	1030							
454.calculix	64	606	871	612	863	**607**	**870**							
459.GemsFDTD	64	1781	381	1688	402	**1690**	**402**							
465.tonto	64	800	787	**793**	**794**	792	796							
470.lbm	64	2279	386	**2220**	**396**	2216	397							
481.wrf	64	944	758	904	791	**917**	**780**							
482.sphinx3	64	1845	676	**1777**	**702**	1738	718							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The config file option 'submit' was used with taskset
to bind processes to cores
```

Platform Notes

```
BIOS Settings
   Hyper-Threading Technology set to ON.
   Turbo Boost was set to 'Disabled'.
ScaleMP
   vSMP Foundation: 2.0.44
Other Cache:
   ScaleMP vSMP Foundation manages cache coherency between the
   InfiniBand-connected systems via multiple concurrent memory
   coherency mechanisms, on a per-block basis, based on
```

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Platform Notes (Continued)

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      real-time memory activity access patterns.
      This mechanism reserves 20GB of the main memory across all
      boards (distributed), which is used as a 4th level cache.
   Hardware Details:
      System was aggregated using 4 X Supermicro SuperServer 6026T-NTR+.
      The servers were connected with Mellanox InfiniBand QDR HCAs and
      a QDR switch.
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Fortran benchmarks:
`ifort`

Benchmarks using both Fortran and C:
`icc ifort`

Base Portability Flags

410.bwaves:	-DSPEC_CPU_LP64
416.gamess:	-DSPEC_CPU_LP64
433.milc:	-DSPEC_CPU_LP64
434.zeusmp:	-DSPEC_CPU_LP64
435.gromacs:	-DSPEC_CPU_LP64 -nofor_main
436.cactusADM:	-DSPEC_CPU_LP64 -nofor_main
437.leslie3d:	-DSPEC_CPU_LP64
444.namd:	-DSPEC_CPU_LP64
447.dealII:	-DSPEC_CPU_LP64
450.soplex:	-DSPEC_CPU_LP64
453.povray:	-DSPEC_CPU_LP64
454.calculix:	-DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD:	-DSPEC_CPU_LP64
465.tonto:	-DSPEC_CPU_LP64
470.lbm:	-DSPEC_CPU_LP64
481.wrf:	-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX -DSPEC_CPU_CASE_FLAG
482.sphinx3:	-DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
`-xSSE4.2 -ipo -O3 -no-prec-div`

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Base Optimization Flags (Continued)

C++ benchmarks:
`-xSSE4.2 -ipo -O3 -no-prec-div`

Fortran benchmarks:
`-xSSE4.2 -ipo -O3 -no-prec-div`

Benchmarks using both Fortran and C:
`-xSSE4.2 -ipo -O3 -no-prec-div`

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic11.0-fp-linux64-revE.20090710.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic11.0-fp-linux64-revE.20090710.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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