Cisco Systems

Cisco UCS B200 M2 (Intel Xeon X5690, 3.46 GHz)

 SPECint®_rate2006 = 416
 SPECint_rate_base2006 = 390

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware

| CPU Name: | Intel Xeon X5690 |
| CPU Characteristics: | Intel Turbo Boost Technology up to 3.73 GHz |
| CPU MHz: | 3467 |
| FPU: | Integrated |
| CPU(s) enabled: | 12 cores, 2 chips, 6 cores/chip, 2 threads/core |
| CPU(s) orderable: | 1,2 chips |
| Primary Cache: | 32 KB I + 32 KB D on chip per core |
| Secondary Cache: | 256 KB I+D on chip per core |
| L3 Cache: | None |
| Other Cache: | None |
| Memory: | 48 GB (12 x 4 GB 2Rx4 PC3L-10600R-9, ECC) |
| Disk Subsystem: | 73 GB SAS, 15K RPM |
| Other Hardware: | None |

Software

| Operating System: | SUSE Linux Enterprise Server 11 (x86_64) with SP1, Kernel 2.6.32.12-0.7-default |
| Compiler: | Intel C++ Compiler XE for applications running on IA-32 |
| Auto Parallel: | No |
| System State: | Run level 3 (multi-user) |
| Base Pointers: | 32-bit |
| Peak Pointers: | 32/64-bit |
| Other Software: | Microquill SmartHeap V9.01 |

Stanard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
Cisco UCS B200 M2 (Intel Xeon X5690, 3.46 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>24</td>
<td>650</td>
<td>361</td>
<td>668</td>
<td>351</td>
<td>653</td>
<td>359</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>24</td>
<td>992</td>
<td>233</td>
<td>1000</td>
<td>232</td>
<td>997</td>
<td>232</td>
</tr>
<tr>
<td>403.gcc</td>
<td>24</td>
<td>745</td>
<td>259</td>
<td>757</td>
<td>255</td>
<td>759</td>
<td>254</td>
</tr>
<tr>
<td>429.mcf</td>
<td>24</td>
<td>723</td>
<td>303</td>
<td>712</td>
<td>308</td>
<td>708</td>
<td>309</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>24</td>
<td>617</td>
<td>408</td>
<td>613</td>
<td>411</td>
<td>623</td>
<td>404</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>24</td>
<td>444</td>
<td>504</td>
<td>443</td>
<td>505</td>
<td>444</td>
<td>504</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>24</td>
<td>742</td>
<td>392</td>
<td>742</td>
<td>391</td>
<td>740</td>
<td>392</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>24</td>
<td>928</td>
<td>572</td>
<td>956</td>
<td>556</td>
<td>986</td>
<td>539</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>24</td>
<td>638</td>
<td>235</td>
<td>638</td>
<td>235</td>
<td>639</td>
<td>235</td>
</tr>
<tr>
<td>473.astar</td>
<td>24</td>
<td>706</td>
<td>239</td>
<td>703</td>
<td>240</td>
<td>704</td>
<td>239</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>24</td>
<td>438</td>
<td>378</td>
<td>438</td>
<td>378</td>
<td>439</td>
<td>377</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The config file option 'submit' was used.
umactl was used to bind copies to the cores

Operating System Notes
ulimit -s unlimited was used to set the stacksize to unlimited prior to run
Large pages were not enabled for this run

Platform Notes
BIOS Configuration : Data Reuse Optimization = Disabled

Base Compiler Invocation
C benchmarks:
   icc -m32
C++ benchmarks:
icpc -m32
Cisco Systems
Cisco UCS B200 M2 (Intel Xeon X5690, 3.46 GHz)

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>416</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>390</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2011
Hardware Availability: Mar-2011
Software Availability: Jan-2011

### Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>-DSPEC_CPU_LINUX_IA32</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>-DSPEC_CPU_LINUX</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>-DSPEC_CPU_LINUX</td>
</tr>
</tbody>
</table>

### Base Optimization Flags

#### C benchmarks
- `xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch`
- `-B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT`

#### C++ benchmarks
- `xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs`
- `-L/smartheap -lsmartheap`
- `-B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT`

### Base Other Flags

#### C benchmarks
- `403.gcc -Dalloca=_alloca`

### Peak Compiler Invocation

#### C benchmarks (except as noted below):
- `icc -m32`
  - 400.perlbench: `icc -m64`
  - 401.bzip2: `icc -m64`
  - 456.hmmer: `icc -m64`
  - 458.sjeng: `icc -m64`

#### C++ benchmarks:
- `icpc -m32`

### Peak Portability Flags
- `400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
- `401.bzip2: -DSPEC_CPU_LP64`

Continued on next page
Cisco Systems
Cisco UCS B200 M2 (Intel Xeon X5690, 3.46 GHz)

SPEC_CINT2006 Result

SPECint_rate2006 = 416
SPECint_rate_base2006 = 390

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2011
Hardware Availability: Mar-2011
Software Availability: Jan-2011

Peak Portability Flags (Continued)

456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -prof-use (pass 2)
        -B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

401.bzip2: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -opt-prefetch -auto-ilp32 -ansi-alias
        -B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div
        -B /usr/share/libhugetlbfs/ -Wl,-hugetlbfs-link=BDT

429.mcf: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -ansi-alias -auto-ilp32

445.gobmk: -xSSE4.2 (pass 2) -prof-gen (pass 1) -prof-use (pass 2)
        -ansi-alias -auto-ilp32

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
        -B /usr/share/libhugetlbfs/ -Wl,-melf_x86_64 -Wl,-hugetlbfs-link=BDT

458.sjeng: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -ansi-alias
        -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -ansi-alias -opt-ra-region-strategy=block
        -L/smartheap -lsmartheap

Continued on next page
Cisco Systems
Cisco UCS B200 M2 (Intel Xeon X5690, 3.46 GHz)

SPECint_rate2006 = 416
SPECint_rate_base2006 = 390

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Feb-2011
Tested by: Cisco Systems
Hardware Availability: Mar-2011
Software Availability: Jan-2011

Peak Optimization Flags (Continued)
473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags
C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.0-linux64-revB.html
http://www.spec.org/cpu2006/flags/Intel-Platform-Settings.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.0-linux64-revB.xml
http://www.spec.org/cpu2006/flags/Intel-Platform-Settings.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.1.
Originally published on 24 March 2011.