# SPEC® CFP2006 Result

**Cisco Systems**  
Cisco UCS C460 M4 (Intel Xeon E7-4850 v2 @ 2.30GHz)  

<table>
<thead>
<tr>
<th>SPECfp®_rate2006</th>
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<tr>
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**CPU2006 license:** 9019  
**Test date:** Mar-2014  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Hardware Availability:** Apr-2014  
**Software Availability:** Sep-2013

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<table>
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<tr>
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<tr>
<td>416.gamess</td>
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<td>433.milc</td>
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<td>434.zeusmp</td>
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<td>435.gromacs</td>
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<td>436.cactusADM</td>
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<td>437.leslie3d</td>
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<td>444.namd</td>
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<td>481.wrf</td>
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<td>482.sphinx3</td>
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Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"
Cisco Systems
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Platform Notes

CPU performance set to Enterprise
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State Cl Enhanced set to Disabled
Package C State Limit set to C0/C1 State
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d10257265a6e4d596a3cee98f191
running on localhost.localdomain Sat Mar 1 00:49:47 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E7-4850 v2 @ 2.30GHz
4 "physical id" (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24

physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 13
cache size : 24576 KB

From /proc/meminfo

MemTotal: 529137472 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)

Non-Compliant
SPEC CFP2006 Result

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Platform Notes (Continued)

From /etc/*release*/etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:
Linux localhost.localdomain 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Feb 28 09:34
SPEC is set to: /opt/cpu2006-1.2

Filesystem Type Used% Mounted on
/dev/sda2 ext4 549G 112G 410G 22% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C460M4.1.5.5.14.020320142203 02/03/2014
Memory:
64x 8 GB
64x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
32x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>
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Base Compiler Invocation

C benchmarks:
icc  -m64

C++ benchmarks:
icpc  -m64

Fortran benchmarks:
ifort  -m64

Benchmarks using both Fortran and C:
icc  -m64 ifort  -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
465.tonto: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphmnx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xAVX  -ipo  -03  -no-prec-div  -opt-prefetch  -auto-p32  -ansi-alias
-opt-mem-layout-trans=3

Continued on next page
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Base Optimization Flags (Continued)

C++ benchmarks:
- xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
- opt-mem-layout-trans=3
Fortran benchmarks:
- xAVX -ipo -O3 -no-prec-div -opt-prefetch
Benchmarks using both Fortran and C:
- xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
- opt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64
482.sphinx3: icc -m32
C++ benchmarks (except as noted below):
icpc -m64
450.soplex: icpc -m32
Fortran benchmarks:
ifort -m64
Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64

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Peak Portability Flags (Continued)

433.milc: -DSPEC_CPU_LP64
434.ezemosmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64
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459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

433.milc: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
          -no-prec-div(pass 2) -auto-ilp32

470.lbm: -xpeep = yes

482.sphinx3: -xAVX -ipo -O3 -no-prec-div -opt-mem-layout-trans=3
             -unroll2

C++ benchmarks:

434.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -fno-alias -auto-ilp32

447.dealII: basepeak = yes

450.soplex: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
           -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
           -prof-use(pass 2) -opt-malloc-options=3

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Peak Optimization Flags (Continued)

453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ips(pass 2) -O3(pass 2)
- no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
- prof-use(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -xAVX(pass 2) - prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
- no-prec-div(pass 2) -prof-use(pass 2) -unroll2
- inline-level=8 - scalar-reg

434.zeusmp: basepeak = yes
437.leslie3d: -xAVX -ipo -O3 -no-prec-div -opt-prefetch

459.GemsFDTD: basepeak = yes
465.tonto: -xAVX(pass 2) - prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
- no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto
- inline-level=8 - scalar-reg - opt-malloc-options=3

Benchmarks using both Fortran and C:
455.gromacs: -xAVX(pass 2) - prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
- no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
- prof-use(pass 2) - opt-prefetch - auto-ilkp32

459.calculix: basepeak = yes
461.lammps: basepeak = yes
455.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.html

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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.xml

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For other inquiries, please contact webmaster@spec.org.

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