Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

SPECint\_rate2006 = 995
SPECint\_rate\_base2006 = 946

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
---
CPU Name: Intel Xeon E5-2650L v4
CPU Characteristics: Intel Turbo Boost Technology up to 2.50 GHz
CPU MHz: 1700
FPU: Integrated
CPU(s) enabled: 28 cores, 2 chips, 14 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 35 MB I+D on chip per chip
Other Cache: None
Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2400T-R)
Disk Subsystem: 1 x 400 GB SSD SAS
Other Hardware: None

Software
---
Operating System: SUSE Linux Enterprise Server 12 SP1 (x86_64) 3.12.49-11-default
Compiler: C/C++ Version 16.0.0.101 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2

---

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Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
CPU performance set to Enterprise
Power Technology set to Performance
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
Memory Power Saving Mode set to Disabled
QPI Snoop Mode set to Cluster-on-Die
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-wg2b Mon Apr 11 10:59:33 2016

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2650L v4@ 1.70GHz
Continued on next page
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Platform Notes (Continued)

2 "physical id"s (chips)
56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 14
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
cache size : 17920 KB

From /proc/meminfo
MemTotal: 264402608 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 1
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP1"
VERSION_ID="12.1" PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp1"

uname -a:
(8d714a0) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 11 10:55

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 14G 546G 3% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M4.3.1.2a.0.022620161405 02/26/2016
Memory:
8x 0xCE00 M393A2G40DB1-CRC 16 GB 2 rank 2400 MHz

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Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

| SPECint_rate2006 = | 995 |
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2016
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Platform Notes (Continued)

8x 0xCE00 M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7.1
Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
  echo 1> /proc/sys/vm/drop_caches
runcspec command invoked through numactl i.e.:
  numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
  icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

C++ benchmarks:
  icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

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**CPU2006 license:** 9019
**Test sponsor:** Cisco Systems
**Test date:** Apr-2016
**Hardware Availability:** Apr-2016
**Tested by:** Cisco Systems
**Software Availability:** Dec-2015

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**Base Optimization Flags**

- C benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
  -opt-mem-layout-trans=3

- C++ benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
  -opt-mem-layout-trans=3 -W1,-z,muldefs -L/sh -lsmartheap

---

**Base Other Flags**

- C benchmarks:
  403.gcc: -Dalloca=_alloca

---

**Peak Compiler Invocation**

- C benchmarks (except as noted below):
  400.perlbench: icc -m64
  401.bzip2: icc -m64
  456.hmmer: icc -m64
  458.sjeng: icc -m64

- C++ benchmarks:
  icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

---

**Peak Portability Flags**

- 400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
- 401.bzip2: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
- 403.gcc: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
- 429.mcf: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
- 445.gobmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
- 456.hmmer: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
- 458.sjeng: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
- 462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
- 464.h264ref: -D_FILE_OFFSET_BITS=64
- 471.omnetpp: -D_FILE_OFFSET_BITS=64
- 473.astar: -D_FILE_OFFSET_BITS=64

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Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

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Peak Portability Flags (Continued)

483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -auto-ilp32

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -opt-prefetch
-auto-ilp32 -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-prof-use(pass 2) -par-num-threads=1(pass 1) -ansi-alias
-opt-mem-layout-trans=3

456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll14
-auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll12
-ansi-alias

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -ansi-alias
-opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
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Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.xml

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