**Cisco Systems**
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECfp®2006</th>
<th>SPECfp_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>95.5</td>
<td>89.7</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019  
**Test date:** Apr-2016  
**Hardware Availability:** Apr-2016  
**Test sponsor:** Cisco Systems  
**Software Availability:** Dec-2015  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>Test Number</th>
<th>Benchmark Name</th>
<th>Result</th>
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<tbody>
<tr>
<td>SPECfp2006</td>
<td>410.bwaves</td>
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<td>416.gamess</td>
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<td>433.milc</td>
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<td></td>
<td>434.zeusmp</td>
<td>173</td>
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<td>435.gromacs</td>
<td>31.9</td>
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<td></td>
<td>436.cactusADM</td>
<td>739</td>
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<tr>
<td></td>
<td>437.leslie3d</td>
<td>284</td>
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<td>22.7</td>
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<td>447.dealII</td>
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<td>465.tonto</td>
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<td>470.lbm</td>
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<tr>
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<td>481.wrf</td>
<td>85.7</td>
</tr>
<tr>
<td></td>
<td>482.sphinx3</td>
<td>50.4</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon E5-2650L v4  
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.50 GHz  
- **CPU MHz:** 1700  
- **FPU:** Integrated  
- **CPU(s) enabled:** 28 cores, 2 chips, 14 cores/chip  
- **CPU(s) orderable:** 1.2 chips  
- **Primary Cache:** 32 KB I + 32 KB D on chip per core  
- **Secondary Cache:** 256 KB I+D on chip per core

**Software**

- **Operating System:** SUSE Linux Enterprise Server 12 SP1 (x86_64) 3.12.49-11-default  
- **Compiler:** C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux; Fortran: Version 16.0.0.101 of Intel Fortran Studio XE for Linux  
- **Auto Parallel:** Yes  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)

Continued on next page
**SPEC CFP2006 Result**

### Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>447.dealII</td>
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<td>465.tonto</td>
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<td>482.sphinx3</td>
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<td><strong>387</strong></td>
<td><strong>50.4</strong></td>
<td>388</td>
<td>50.2</td>
</tr>
</tbody>
</table>

**Software Availability:** Dec-2015

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

BIOS Settings:
- Intel Hyper-Threading Technology option set to Disabled
- CPU performance set to Enterprise
- Power Technology set to Energy Efficient
- Energy Performance BIAS setting set to Balanced Performance
- Memory RAS configuration set to Maximum Performance
- Memory Power Saving Mode set to Disabled
- QPI Snoop Mode set to Home Directory Snoop with OSB

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)  

**SPECfp2006 =** 95.5  
**SPECfp_base2006 =** 89.7

<table>
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<tr>
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<th>9019</th>
<th>Test date:</th>
<th>Apr-2016</th>
</tr>
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<tbody>
<tr>
<td>Test sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2016</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Dec-2015</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

running on linux-wg2b Tue Apr 19 17:21:34 2016

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) CPU E5-2650L v4@ 1.70GHz
  2 "physical id"s (chips)
  28 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 14
  siblings : 14
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
  cache size : 35840 KB
```

From /proc/meminfo

```
MemTotal:       264406532 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From /etc/*release* /etc/*version*

```
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 1
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP1"
    VERSION_ID="12.1"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp1"
```

uname -a:

```
(8d714a0) x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Apr 19 10:06
```

SPEC is set to: /opt/cpu2006-1.2

<table>
<thead>
<tr>
<th>Filesystem Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use% Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>559G</td>
<td>12G</td>
<td>547G</td>
</tr>
</tbody>
</table>

Additional information from dmidecode:

Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

**SPEC CFP2006 Result**

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**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Test date:** Apr-2016  
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**Software Availability:** Dec-2015

**Platform Notes (Continued)**

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M4.3.1.2a.0.022620161405 02/26/2016
Memory:
- 8x 0xCE00 M393A2G40DB1-CRC 16 GB 2 rank 2400 MHz
- 8x 0xCE00 M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz
- 8x NO DIMM NO DIMM

(End of data from sysinfo program)

**General Notes**

Environment variables set by runspec before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib32:/opt/cpu2006-1.2/lib64:/opt/cpu2006-1.2/sh"
- OMP_NUM_THREADS = "28"

Binaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7.1
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

**Base Compiler Invocation**

C benchmarks:
- icc -m64

C++ benchmarks:
- icpc -m64

Fortran benchmarks:
- ifort -m64

Benchmarks using both Fortran and C:
- icc -m64 ifort -m64

**Base Portability Flags**

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main

Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

SPECfp2006 = 95.5
SPECfp_base2006 = 89.7

CPU2006 license: 9019
Test date: Apr-2016
Test sponsor: Cisco Systems
Hardware Availability: Apr-2016
Tested by: Cisco Systems
Software Availability: Dec-2015

Base Portability Flags (Continued)

436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch
-ansi-alias

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch -ansi-alias

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch
-ansi-alias

Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

SPECfp2006 = 95.5
SPECfp_base2006 = 89.7

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -fno-alias
-auto-ilp32
447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll4
-ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll2
-inline-level=0 -scalar-rep-
434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll2
-inline-level=0 -opt-prefetch -parallel
465.tonto: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -inline-calloc
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650L v4, 1.70 GHz)

SPECfp2006 = 95.5
SPECfp_base2006 = 89.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2016
Hardware Availability: Apr-2016
Software Availability: Dec-2015

Peak Optimization Flags (Continued)

465.tonto (continued):
-opty-malloc-options=3 -auto -unroll4

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes

454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32 -ansi-alias

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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