### SPECint® Rate 2006

**Result**

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6142 2.60GHz)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint® Rate 2006</td>
<td>3540</td>
</tr>
<tr>
<td>SPECint Rate Base 2006</td>
<td>3360</td>
</tr>
</tbody>
</table>

**CPU 2006 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested By:** Cisco Systems
**Test Date:** Aug-2017
**Hardware Availability:** Aug-2017
**Software Availability:** Apr-2017

#### Software

- **Operating System:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
- **Auto Parallel:** Yes
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 32-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** Microquill SmartHeap V10.2

#### Hardware

- **CPU Name:** Intel Xeon Gold 6142
- **CPU Characteristics:** Intel Turbo Boost Technology up to 3.70 GHz
- **CPU MHz:** 2600
- **FPU:** Integrated
- **CPU(s) enabled:** 64 cores, 4 chips, 16 cores/chip, 2 threads/core
- **CPU(s) orderable:** 2,4 chips
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 1 MB I+D on chip per core
- **L3 Cache:** 22 MB I+D on chip per chip
- **Memory:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- **Other Cache:** None
- **Disk Subsystem:** 1 x 1 TB SAS HDD, 7.2K RPM
- **Other Hardware:** None

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<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>2940</td>
</tr>
<tr>
<td>bzip2</td>
<td>1480</td>
</tr>
<tr>
<td>gcc</td>
<td>2370</td>
</tr>
<tr>
<td>mcf</td>
<td>3540</td>
</tr>
<tr>
<td>gobmk</td>
<td>2060</td>
</tr>
<tr>
<td>hammer</td>
<td>5630</td>
</tr>
<tr>
<td>sjeng</td>
<td>2340</td>
</tr>
<tr>
<td>libquantum</td>
<td>2360</td>
</tr>
<tr>
<td>h264ref</td>
<td>2060</td>
</tr>
<tr>
<td>omnetpp</td>
<td>1880</td>
</tr>
<tr>
<td>astar</td>
<td>1860</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>3870</td>
</tr>
</tbody>
</table>

**SPECint Rate Base 2006 = 3360**

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**Brainstorming:**

- Consider using the Intel Xeon Gold 6142 processor for higher performance.
- The system has a peak memory of 768 GB, which can support large-scale computations.

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**Conclusion:**

Cisco UCS C480 M5 with Intel Xeon Gold 6142 processors performs well in SPECint tests, achieving a high SPECint Rate 2006 of 3540. The system is well-equipped for computational tasks, with ample memory and high-speed processors.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142 2.60GHz)

SPECint_rate2006 = 3540
SPECint_rate_base2006 = 3360

CPU2006 license: 9019
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Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>128</td>
<td>502</td>
<td>2490</td>
<td>503</td>
<td>2490</td>
<td>502</td>
<td>2490</td>
<td>128</td>
<td>420</td>
<td>2980</td>
<td>419</td>
<td>2980</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>128</td>
<td>833</td>
<td>1480</td>
<td>837</td>
<td>1480</td>
<td>834</td>
<td>1480</td>
<td>128</td>
<td>794</td>
<td>1560</td>
<td>801</td>
<td>1540</td>
</tr>
<tr>
<td>403.gcc</td>
<td>128</td>
<td>437</td>
<td>2360</td>
<td>436</td>
<td>2360</td>
<td>434</td>
<td>2360</td>
<td>128</td>
<td>257</td>
<td>4540</td>
<td>257</td>
<td>4540</td>
</tr>
<tr>
<td>429.mcf</td>
<td>128</td>
<td>651</td>
<td>2060</td>
<td>652</td>
<td>2060</td>
<td>650</td>
<td>2060</td>
<td>128</td>
<td>212</td>
<td>5640</td>
<td>212</td>
<td>5640</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>128</td>
<td>260</td>
<td>4600</td>
<td>258</td>
<td>4600</td>
<td>259</td>
<td>4600</td>
<td>128</td>
<td>257</td>
<td>4540</td>
<td>257</td>
<td>4540</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>128</td>
<td>699</td>
<td>2210</td>
<td>700</td>
<td>2210</td>
<td>699</td>
<td>2210</td>
<td>128</td>
<td>651</td>
<td>2380</td>
<td>651</td>
<td>2380</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>128</td>
<td>48.5</td>
<td>54700</td>
<td>48.5</td>
<td>54700</td>
<td>48.6</td>
<td>54600</td>
<td>128</td>
<td>48.5</td>
<td>54700</td>
<td>48.5</td>
<td>54700</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>128</td>
<td>750</td>
<td>3780</td>
<td>758</td>
<td>3740</td>
<td>759</td>
<td>3730</td>
<td>128</td>
<td>731</td>
<td>3880</td>
<td>727</td>
<td>3900</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>128</td>
<td>474</td>
<td>1690</td>
<td>475</td>
<td>1690</td>
<td>475</td>
<td>1680</td>
<td>128</td>
<td>439</td>
<td>1820</td>
<td>440</td>
<td>1820</td>
</tr>
<tr>
<td>473.astar</td>
<td>128</td>
<td>483</td>
<td>1860</td>
<td>482</td>
<td>1860</td>
<td>483</td>
<td>1860</td>
<td>128</td>
<td>483</td>
<td>1860</td>
<td>482</td>
<td>1860</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>128</td>
<td>229</td>
<td>3860</td>
<td>228</td>
<td>3870</td>
<td>228</td>
<td>3870</td>
<td>128</td>
<td>229</td>
<td>3860</td>
<td>228</td>
<td>3870</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
runtime on linux-p0v5 Fri Aug 25 03:54:17 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142
2.60GHz)

SPECint_rate2006 = 3540
SPECint_rate_base2006 = 3360

CPU2006 license: 9019
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Platform Notes (Continued)

4 "physical id"s (chips)
128 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

cache size : 22528 KB

From /proc/meminfo
MemTotal: 791191800 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-p0v5 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464/f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 24 10:58

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 930G 11G 920G 2% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017

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Platform Notes (Continued)
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "~/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation
C benchmarks:
  icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
C++ benchmarks:
  icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags
400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
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**SPEC CINT2006 Result**

**SPECint_rate2006 = 3540**

**SPECint_rate_base2006 = 3360**

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- **Test date:** Aug-2017
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**Base Optimization Flags**

C benchmarks:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3
```

C++ benchmarks:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap
```

---

**Base Other Flags**

C benchmarks:
```
403.gcc: -Dalloca=_alloca
```

---

**Peak Compiler Invocation**

C benchmarks (except as noted below):
```
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:
```
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

---

**Peak Portability Flags**

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64

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Peak Portability Flags (Continued)
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags
C benchmarks:
400.perlbench: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
- qopt-mem-layout-trans=3

403.gcc: 
-xCORE-AVX512 -ipo -03 -no-prec-div
- qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: 
-xCORE-AVX512 -ipo -03 -no-prec-div -unroll2 -auto-ilp32
- qopt-mem-layout-trans=3

458.sjeng: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2) -unroll4 -auto-ilp32
- qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:
471.omnetpp: 
- prof-gen(pass 1) - prof-use(pass 2) -xCORE-AVX512(pass 2)
- par-num-threads=1(pass 1) -ipo(pass 2) -03(pass 2)
- no-prec-div(pass 2)
- qopt-ra-region-strategy=block
- qopt-mem-layout-trans=3 -Wl,-z,muldefs
- L/sh10.2 -lsmartheap

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Peak Optimization Flags (Continued)

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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