## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**Test Date:** Oct-2017  
**Hardware Availability:** Oct-2017  
**Software Availability:** Sep-2017

### CPU2017 Floating Point Speed Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Average</th>
<th>Standard Deviation</th>
<th>SPECspeed2017_fp_base</th>
<th>SPECspeed2017_fp_peak</th>
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<tr>
<td>603.bwaves_s</td>
<td>259</td>
<td>16</td>
<td>188</td>
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<td>607.cactuBSSN_s</td>
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<td>627.cam4_s</td>
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<td>628.pop2_s</td>
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<tr>
<td>638.imagick_s</td>
<td>247</td>
<td>10</td>
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<tr>
<td>644.nab_s</td>
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<td>654.roms_s</td>
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<td>10</td>
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</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Platinum 8180
- **Max MHz.:** 3800
- **Nominal:** 2500
- **Enabled:** 112 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 38.5 MB I+D on chip per chip
- **Memory:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 480 GB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.1 released Oct-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

SPECspeed2017_fp_base = 188
SPECspeed2017_fp_peak = 190

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>315</td>
<td>55.3</td>
<td>285</td>
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<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

SPECspeed2017_fp_base = 188
SPECspeed2017_fp_peak = 190

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

running on C480-SLES12 Mon Oct  2 22:15:14 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
  4 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                112
On-line CPU(s) list:   0-111
Thread(s) per core:    1
Core(s) per socket:    28
Socket(s):             4
NUMA node(s):          4
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
Stepping:              4
CPU MHz:               1026.614
CPU max MHz:           3800.0000
CPU min MHz:           1000.0000
BogoMIPS:              5000.19
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              39424K

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

**SPEC CPU2017 Floating Point Speed Result**

**Specspeed2017_fp_base** = 188
**Specspeed2017_fp_peak** = 190

---

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Test Date:** Oct-2017
**Hardware Availability:** Oct-2017
**Software Availability:** Sep-2017

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**Platform Notes (Continued)**

NUMA node0 CPU(s): 0-27
NUMA node1 CPU(s): 28-55
NUMA node2 CPU(s): 56-83
NUMA node3 CPU(s): 84-111

Flags:

```
fpu vme de pse tsc msr pae mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwlp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnum flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsaves
xgetbv1 cqm_llc cqm_occup_llc
```

/proc/cpuinfo cache data

```
cache size : 39424 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 192015 MB
node 0 free: 190214 MB
node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
53 54 55
node 1 size: 193521 MB
node 1 free: 191130 MB
node 2 cpus: 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
81 82 83
node 2 size: 193521 MB
node 2 free: 191759 MB
node 3 cpus: 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105
106 107 108 109 110 111
node 3 size: 193384 MB
node 3 free: 192227 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10
```

From /proc/meminfo

```
MemTotal: 790981780 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

SPEC CPU2017 Floating Point Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

SPECspeed2017_fp_base = 188
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Cisco Systems

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Tested by: Cisco Systems
Test Date: Oct-2017
Hardware Availability: Oct-2017
Software Availability: Sep-2017

Platform Notes (Continued)

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux C480-SLES12 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Oct 2 21:11

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda3 xfs 404G 65G 340G 17% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. C480M5.3.1.0.272.0613172154 06/13/2017
  Memory:
    48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

  (End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

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Compiler Version Notes (Continued)

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CC  619.lbm_s(peak)

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  607.cactuBSSN_s(base)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  607.cactuBSSN_s(peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

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FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

cc 621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)
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Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
iccc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)

654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)  

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</table>

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

- 619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2
- ipopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
- ipopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
- DSPEC_OPENMP

- 638.imagick_s: -xCORE-AVX2 -ipo -O3 -qopt-prefetch
- ipopt-mem-layout-trans=3 -qopenmp
- DSPEC_OPENMP

- 644.nab_s: Same as 638.imagick_s

Fortran benchmarks:

- -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
- DSPEC_OPENMP -O2 -xCORE-AVX2 -qopt-prefetch -ipo -O3
- ipopt-mem-layout-trans=3 -qopenmp
- nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

- 621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2
- qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
- qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180, 2.50GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

621.wrf_s (continued):
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX2 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2 -gopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -gopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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