## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6150, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 8.81</th>
<th>SPECspeed®2017_int_peak = 9.09</th>
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<tr>
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<td><strong>Software Availability:</strong> Sep-2017</td>
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</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6150  
- **Max MHz:** 3700  
- **Nominal:** 2700  
- **Enabled:** 36 cores, 2 chips  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 24.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)  
- **Storage:** 1 x 300 GB SAS SSD  
- **Other:** None  

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
  4.4.21-69-default  
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;  
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 3.2.1d released Jul-2017  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc: jemalloc memory allocator library v5.0.1;  
  jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;  
  jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;  
  jemalloc: sources available from jemalloc.net or releases  
- **Power Management:** --

### SPEC CPU 2017 Integer Speed Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads (9.09)</th>
<th>SPECspeed®2017_int_base (8.81)</th>
<th>SPECspeed®2017_int_peak (9.09)</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>6.20</td>
<td>7.59</td>
<td>9.26</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>6.42</td>
<td>6.22</td>
<td>9.53</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>6.42</td>
<td>6.22</td>
<td>10.9</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>6.42</td>
<td>6.22</td>
<td>11.0</td>
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<tr>
<td>623.xalancbmk_s</td>
<td>6.42</td>
<td>6.22</td>
<td>9.48</td>
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<tr>
<td>625.x264_s</td>
<td>6.42</td>
<td>6.22</td>
<td>10.2</td>
</tr>
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<td>631.deepsjeng_s</td>
<td>6.42</td>
<td>6.22</td>
<td>11.8</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>6.42</td>
<td>6.22</td>
<td>5.05</td>
</tr>
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<td>648.exchange2_s</td>
<td>6.42</td>
<td>6.22</td>
<td>11.8</td>
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<td>6.42</td>
<td>6.22</td>
<td>22.1</td>
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Ratio</th>
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<td>22.1</td>
<td>282</td>
<td>21.9</td>
<td>280</td>
<td>22.1</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto

(Continued on next page)
### Platform Notes (Continued)

Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux Sat Sep 30 11:55:07 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
  2 "physical id"s (chips)
36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
Stepping: 4
CPU MHz: 2701.000
CPU max MHz: 2701.0000
CPU min MHz: 1200.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov

(Continued on next page)
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Cisco UCS B200 M5 (Intel Xeon Gold 6150, 2.70GHz)

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Platform Notes (Continued)

pat pse36 clflush dts acpi mmx fxsr sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmerge eagerfpui pni pclmulqdq dtes64 monitor ds_cpl vsx est tm2 ssse3 sdbg
fma cx16 xpmr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm intel_pt
tpr_shadow vmvi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2
erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
  node 0 size: 385449 MB
  node 0 free: 376425 MB
  node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
  node 1 size: 387040 MB
  node 1 free: 378725 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791029236 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

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Platform Notes (Continued)

uname -a:
Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67) x86_64
x86_64 x86_64 GNU/Linux
run-level 3 Jan 18 22:57
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 90G 190G 33% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
Fortran | 648.exchange2_s(base, peak)
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6150, 2.70GHz)

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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
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Base Other Flags

C benchmarks:
- -m64 -std=c11

C++ benchmarks:
- -m64

Fortran benchmarks:
- -m64

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

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Peak Optimization Flags (Continued)

600.perlbench_s (continued):
-DSPEC_OPENMP -fno-strict-overflow
-\-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: \-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: \-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-\-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: \-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-\-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: \-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-\-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: \-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-\-L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-\-L/usr/local/je5.0.1-64/lib -ljemalloc
# SPEC CPU®2017 Integer Speed Result

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### SPECspeed®2017 Results

- **SPECspeed®2017_int_base = 8.81**
- **SPECspeed®2017_int_peak = 9.09**

## Peak Other Flags

**C benchmarks:**
- `-m64 -std=c11`

**C++ benchmarks (except as noted below):**
- `-m64`

- `623.xalancbmk_s: -m32`

**Fortran benchmarks:**
- `-m64`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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