Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPECspeed2017_fp_base = 121
SPECspeed2017_fp_peak = 122

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Threads

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<td>44.1</td>
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<tr>
<td>621.wrf_s</td>
<td>99.3</td>
<td>164</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>91.2</td>
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<tr>
<td>628.pop2_s</td>
<td>73.5</td>
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<td>644.nab_s</td>
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<tr>
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</tr>
<tr>
<td>654.roms_s</td>
<td>119</td>
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SPECspeed2017_fp_base (121) SPECspeed2017_fp_peak (122)

Hardware
CPU Name: Intel Xeon Gold 6154
Max MHz.: 3700
Nominal: 3000
Enabled: 36 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per core
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++
Compiler for Linux:
Fortran: Version 18.0.0.128 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.1d released Sep-2017
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPECspeed2017_fp_base = 121
SPECspeed2017_fp_peak = 122

Results Table

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<td>120</td>
<td>129</td>
<td>122</td>
<td>130</td>
<td>121</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Files system page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

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<tr>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

running on linux-3u87 Sat Sep 30 17:20:14 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6154 CPU @ 3.00GHz
  2 "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6154 CPU @ 3.00GHz
Stepping: 4
CPU MHz: 1300.000
CPU max MHz: 3001.0000
CPU min MHz: 1200.0000
BogoMIPS: 5999.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mxr ssse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
ldtsc plconstant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitord s_cpl vmx smx est tm2 ssse3 sdbg

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 121
SPECspeed2017_fp_peak = 122

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm intel_pt
tpr_shadow vmmi flexpriority ept vpid fs.gsbase tsc_adjust bmi1 hle avx2 smep bmi2
erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx clflushopt clwb avx512cd
avx512bw avx512vl xsavesopt xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data
  cache size: 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
  node 0 size: 192074 MB
  node 0 free: 183346 MB
  node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
  node 1 size: 193504 MB
  node 1 free: 179245 MB
  node distances:
    node  0   1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 394832580 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

  uname -a:
    Linux linux-3u87 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPECspeed2017_fp_base = 121
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Hardware Availability: Aug-2017
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Platform Notes (Continued)

run-level 3 Jan 18 23:10

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 xfs 224G 66G 158G 30% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory: 24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CC  619.lbm_s(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
FC  607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
FC  607.cactuBSSN_s(peak)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPEC CPU2017 Floating Point Speed Result
Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPECspeed2017_fp_base = 121
SPECspeed2017_fp_peak = 122

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Oct-2017
Hardware Availability: Aug-2017
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Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 603.bwaves_s(peak) 649.fotonik3d_s(peak) 654.roms_s(peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CC 621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CC 621.wrf_s(peak) 628.pop2_s(peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

<table>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Base Compiler Invocation (Continued)

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```

### Base Portability Flags

- 603.bwaves_s: -DSPEC_LP64  
- 607.cactuBSSN_s: -DSPEC_LP64  
- 619.lbm_s: -DSPEC_LP64  
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG  
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl  
- 638.imagick_s: -DSPEC_LP64  
- 644.nab_s: -DSPEC_LP64  
- 649.fotonik3d_s: -DSPEC_LP64  
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

```
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

**Fortran benchmarks:**

```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp  
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPEC\texttabular{fp_base}{= 121}
SPEC\texttabular{fp_peak}{= 122}

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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-\texttt{nostandard-realloc-lhs} -\texttt{align array32byte}

Base Other Flags

C benchmarks:
-\texttt{m64} \texttt{-std=c11}

Fortran benchmarks:
-\texttt{m64}

Benchmarks using both Fortran and C:
-\texttt{m64} \texttt{-std=c11}

Benchmarks using Fortran, C, and C++:
-\texttt{m64} \texttt{-std=c11}

Peak Compiler Invocation

C benchmarks:
\texttt{icc}

Fortran benchmarks:
\texttt{ifort}

Benchmarks using both Fortran and C:
\texttt{ifort icc}

Benchmarks using Fortran, C, and C++:
\texttt{icpc icc ifort}

Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)

SPECspeed2017_fp_base = 121
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CPU2017 License: 9019
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Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prog-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prog-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

(Continued on next page)
## Cisco Systems

**Cisco UCS B200 M5 (Intel Xeon Gold 6154, 3.00GHz)**

<table>
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</tr>
</tbody>
</table>

### Peak Other Flags (Continued)

Fortran benchmarks:
- `-m64`

Benchmarks using both Fortran and C:
- `-m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11`

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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