**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 5120</td>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
</tr>
<tr>
<td>Max MHz: 3200</td>
<td>Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Nominal: 2200</td>
<td>Parallel: Yes</td>
</tr>
<tr>
<td>Enabled: 28 cores, 2 chips</td>
<td>Firmware: Version 3.2.1d released Jul-2017</td>
</tr>
<tr>
<td>Orderable: 1.2 Chips</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 19.25 MB I+D on chip per chip</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases</td>
</tr>
<tr>
<td>Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)</td>
<td>Power Management: --</td>
</tr>
<tr>
<td>Storage: 1 x 1 TB SAS HDD, 7.2K RPM</td>
<td></td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Integer Speed Result**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

<table>
<thead>
<tr>
<th>Thread</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>6.40</td>
<td>8.22</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>8.47</td>
<td>9.99</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>5.29</td>
<td>10.0</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>5.57</td>
<td>10.2</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>8.28</td>
<td>10.2</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>4.46</td>
<td>11.6</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>3.76</td>
<td>11.6</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>3.77</td>
<td>19.1</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>8.22</td>
<td>19.2</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>5.39</td>
<td>19.2</td>
</tr>
</tbody>
</table>

**Software**

| Base Pointers: 64-bit |
| Peak Pointers: 32/64-bit |

**Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>28</td>
<td>331</td>
<td>5.37</td>
<td>329</td>
<td>5.40</td>
<td>329</td>
<td>5.39</td>
<td>28</td>
<td>276</td>
<td>6.44</td>
<td>278</td>
<td>6.40</td>
<td>277</td>
<td>6.40</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>28</td>
<td>485</td>
<td>8.22</td>
<td>488</td>
<td>8.16</td>
<td>480</td>
<td>8.29</td>
<td>28</td>
<td>465</td>
<td>8.57</td>
<td>470</td>
<td>8.47</td>
<td>473</td>
<td>8.42</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>28</td>
<td>303</td>
<td>5.38</td>
<td>308</td>
<td>5.29</td>
<td>315</td>
<td>5.17</td>
<td>28</td>
<td>302</td>
<td>5.40</td>
<td>304</td>
<td>5.37</td>
<td>318</td>
<td>5.13</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>28</td>
<td>171</td>
<td>8.28</td>
<td>171</td>
<td>8.28</td>
<td>171</td>
<td>8.27</td>
<td>28</td>
<td>162</td>
<td>8.77</td>
<td>162</td>
<td>8.73</td>
<td>162</td>
<td>8.75</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>28</td>
<td>173</td>
<td>10.2</td>
<td>173</td>
<td>10.2</td>
<td>174</td>
<td>10.2</td>
<td>28</td>
<td>173</td>
<td>10.2</td>
<td>173</td>
<td>10.2</td>
<td>173</td>
<td>10.2</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>28</td>
<td>320</td>
<td>4.48</td>
<td>321</td>
<td>4.46</td>
<td>321</td>
<td>4.46</td>
<td>28</td>
<td>322</td>
<td>4.45</td>
<td>321</td>
<td>4.46</td>
<td>321</td>
<td>4.46</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>28</td>
<td>454</td>
<td>3.76</td>
<td>454</td>
<td>3.76</td>
<td>454</td>
<td>3.76</td>
<td>28</td>
<td>452</td>
<td>3.77</td>
<td>453</td>
<td>3.77</td>
<td>453</td>
<td>3.76</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>28</td>
<td>254</td>
<td>11.6</td>
<td>254</td>
<td>11.6</td>
<td>255</td>
<td>11.5</td>
<td>28</td>
<td>255</td>
<td>11.5</td>
<td>254</td>
<td>11.6</td>
<td>254</td>
<td>11.6</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>28</td>
<td>326</td>
<td>18.9</td>
<td>324</td>
<td>19.1</td>
<td>324</td>
<td>19.1</td>
<td>28</td>
<td>322</td>
<td>19.2</td>
<td>322</td>
<td>19.2</td>
<td>322</td>
<td>19.2</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 7.70**
**SPECspeed®2017_int_peak = 7.92**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

- **KMP_AFFINITY = "granularity=fine,scatter"**
- **LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"**
- **OMP_STACKSIZE = "192M"**

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```bash
csync; echo 3> /proc/sys/vm/drop_caches
cmalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5
```

Sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

### Platform Notes

**BIOS Settings:**

- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Disabled
- IMC Interleaving set to Auto

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 7.70
SPECspeed®2017_int_peak = 7.92

CPU2017 License: 9019
Test Date: Oct-2017
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f
running on linux-uezu Sat Sep 30 13:35:47 2017
SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
2 "physical id"s (chips)
28 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 14
siblings : 14
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 28
On-line CPU(s) list: 0-27
Thread(s) per core: 1
Core(s) per socket: 14
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
Stepping: 4
CPU MHz: 1000.000
CPU max MHz: 2201.0000
CPU min MHz: 1000.0000
BogoMIPS: 4399.99
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-13
NUMA node1 CPU(s): 14-27
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov

(Continued on next page)
Platform Notes (Continued)

pat pse36 clflush dts acpi mmx fxsr sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmerf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrr pdcid pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm intel_pt
tpr_shadow vmmi flexpriority ept vpid fgsgsbase tsc_adjust bmi1 hle avx2 smep bmi2
ermi invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13
  node 0 size: 192074 MB
  node 0 free: 181420 MB
  node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  node 1 size: 193504 MB
  node 1 free: 187565 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo

MemTotal: 394832632 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 7.70
SPECspeed®2017_int_peak = 7.92

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Software Availability: Sep-2017
Test Date: Oct-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems

Platform Notes (Continued)

uname -a:
    Linux linux-uezu 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 17 11:23

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 894G 84G 810G 10% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.07271353 07/27/2017
    Memory:
        24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

    (End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
        | 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
        | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

**SPEC CPU®2017 Integer Speed Result**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**SPECspeed®2017_int_base = 7.70**  
**SPECspeed®2017_int_peak = 7.92**  
**Test Date:** Oct-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Base Compiler Invocation

C benchmarks:  
`icc`

C++ benchmarks:  
`icpc`

Fortran benchmarks:  
`ifort`

### Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64

### Base Optimization Flags

C benchmarks:  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/je5.0.1-64/lib -ljemalloc
# SPEC CPU®2017 Integer Speed Result

## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Oct-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2017</td>
</tr>
</tbody>
</table>

### SPECspeed2017_int_base = 7.70

### SPECspeed2017_int_peak = 7.92

## Base Other Flags

C benchmarks:
- m64 -std=c11

C++ benchmarks:
- m64

Fortran benchmarks:
- m64

## Peak Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

## Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

## Peak Optimization Flags

C benchmarks:
- 600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
- xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
- no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPECspeed®2017_int_base = 7.70
SPECspeed®2017_int_peak = 7.92

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Optimization Flags (Continued)

600.perlbench_s (continued):
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:
620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPECspeed®2017_int_base = 7.70
SPECspeed®2017_int_peak = 7.92

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks (except as noted below):
-m64

623.xalancbmk_s: -m32

Fortran benchmarks:
-m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-09-30 13:35:47-0400.
Report generated on 2020-09-03 17:11:52 by CPU2017 PDF formatter v6255.
Originally published on 2017-10-26.