Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed2017_fp_base</th>
<th>SPECspeed2017_fp_peak</th>
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<tr>
<td>603.bwaves_s 28</td>
<td>118</td>
<td>119</td>
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<tr>
<td>607.cactuBSSN_s 28</td>
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<tr>
<td>619.lbm_s 28</td>
<td>65.9</td>
<td>66.6</td>
</tr>
<tr>
<td>621.wrf_s 28</td>
<td>53.4</td>
<td>53.3</td>
</tr>
<tr>
<td>627.cam4_s 28</td>
<td>54.6</td>
<td>53.2</td>
</tr>
<tr>
<td>628.pop2_s 28</td>
<td>73.2</td>
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<tr>
<td>638.imagick_s 28</td>
<td>73.1</td>
<td>73.4</td>
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<tr>
<td>644.nab_s 28</td>
<td>136</td>
<td>136</td>
</tr>
<tr>
<td>649.fotonik3d_s 28</td>
<td>102</td>
<td>107</td>
</tr>
<tr>
<td>654.roms_s 28</td>
<td>SPECspeed2017_fp_base (88.4)</td>
<td>SPECspeed2017_fp_peak (89.1)</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 5120
Max MHz.: 3200
Nominal: 2200
Enabled: 28 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 19.25 MB I+D on chip per core
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
Storage: 1 x 600 GB SAS HDD, 10K RPM
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.1d released Sep-2017
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPECspeed2017_fp_base = 88.4
SPECspeed2017_fp_peak = 89.1

Test Date: Oct-2017
Hardware Availability: Aug-2017
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Results Table

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<td>28</td>
<td>149</td>
<td>106</td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 88.4
SPECspeed2017_fp_peak = 89.1

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b0c091c0f

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)
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SPEC CPU2017 Floating Point Speed Result

**SPECspeed2017_fp_base** = 88.4
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**CPU2017 License**: 9019
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**Test Sponsor**: Cisco Systems
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**Platform Notes (Continued)**

- fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
- xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
- hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi flexpriority ept vpid
- fsqsbosbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqmx mpavx512f
- avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsavexopt xsave
- xgetbv1 cqmx_llc cqmx_occu pp_llc

```
/proc/cpuinfo
```

**cache**

- size : 19712 KB

---

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.

- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13
- node 0 size: 191913 MB
- node 0 free: 188027 MB
- node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27
- node 1 size: 193504 MB
- node 1 free: 189459 MB

---

From `/proc/meminfo`

- MemTotal: 394667556 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

---

From `/etc/*release*` /etc/*version*

**SuSE-release**:

- SUSE Linux Enterprise Server 12 (x86_64)
- VERSION = 12
- PATCHLEVEL = 2
- # This file is deprecated and will be removed in a future service pack or release.
- # Please check /etc/os-release for details about this release.

**os-release**:

- NAME="SLES"
- VERSION="12-SP2"
- VERSION_ID="12.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
- ID="sles"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:12:sp2"

**uname -a**:

```
Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
```

(Continued on next page)
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Platform Notes (Continued)

x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 2 02:20

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 119G 441G 22% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC 619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
==============================================================================

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 607.cactuBSSN_s(base)
==============================================================================

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

SPECspeed2017_fp_base = 88.4
SPECspeed2017_fp_peak = 89.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

FC  607.cactuBSSN_s(peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
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==============================================================================
CC  621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)

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CC  621.wrf_s(peak) 628.pop2_s(peak)

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Base Compiler Invocation

C benchmarks:
icc

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz) | SPECspeed2017_fp_base = 88.4
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**Base Compiler Invocation (Continued)**

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)  

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### Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-gopt-prefetch`  
- `-ffinite-math-only`  
- `-gopt-mem-layout-trans=3`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`

### Base Other Flags

C benchmarks:
- `-m64`  
- `-std=c11`

Fortran benchmarks:
- `-m64`

Benchmarks using both Fortran and C:
- `-m64`  
- `-std=c11`

Benchmarks using Fortran, C, and C++:
- `-m64`  
- `-std=c11`

### Peak Compiler Invocation

C benchmarks:
- `icc`

Fortran benchmarks:
- `ifort`

Benchmarks using both Fortran and C:
- `ifort icc`

Benchmarks using Fortran, C, and C++:
- `icpc icc ifort`

### Peak Portability Flags

Same as Base Portability Flags
Peak Optimization Flags

C benchmarks:

619.lbm_s:  -prof-gen(pass 1)  -prof-use(pass 2)  -O2  -xCORE-AVX512
-ipo -O3  -ffinite-math-only  -no-prec-div
-qopt-mem-layout-trans=3  -DSPEC_SUPPRESS_OPENMP  -qopenmp
-DSPEC_OPENMP

638.imagick_s:  -xCORE-AVX512  -ipo  -O3  -no-prec-div  -qopt-prefetch
-ffinite-math-only  -qopt-mem-layout-trans=3  -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:

-prof-gen(pass 1)  -prof-use(pass 2)  -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP  -O2  -xCORE-AVX512
-qopt-prefetch  -ipo  -O3
-ffinite-math-only  -no-prec-div  -qopt-mem-layout-trans=3  -qopenmp
-nostandard-realloc-lhs  -align array32byte

Benchmarks using both Fortran and C:

621.wrf_s:  -prof-gen(pass 1)  -prof-use(pass 2)  -O2  -xCORE-AVX512
-qopt-prefetch  -ipo  -O3  -ffinite-math-only  -no-prec-div
-qopt-mem-layout-trans=3  -DSPEC_SUPPRESS_OPENMP  -qopenmp
-DSPEC_OPENMP  -nostandard-realloc-lhs  -align array32byte

627.cam4_s:  -xCORE-AVX512  -ipo  -O3  -no-prec-div  -qopt-prefetch
-ffinite-math-only  -qopt-mem-layout-trans=3  -qopenmp
-DSPEC_OPENMP  -nostandard-realloc-lhs  -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

-prof-gen(pass 1)  -prof-use(pass 2)  -O2  -xCORE-AVX512
-ipo  -O3  -ffinite-math-only  -no-prec-div  -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP  -qopenmp  -DSPEC_OPENMP  -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:

-m64  -std=c11

(Continued on next page)
### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

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<thead>
<tr>
<th>SPECspeed2017_fp_peak</th>
<th>SPECspeed2017_fp_base</th>
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### Peak Other Flags (Continued)

Fortran benchmarks:
- `-m64`

Benchmarks using both Fortran and C:
- `-m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11`

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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