## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 5115, 2.40 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 75.3</th>
<th>SPECspeed®2017_fp_peak = 76.0</th>
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<th>9019</th>
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<td>Hardware Availability:</td>
<td>Aug-2017</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 5115  
- **Max MHz:** 3200  
- **Nominal:** 2400  
- **Enabled:** 20 cores, 2 chips  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)  
- **Storage:** 1 x 1 TB SAS HDD, 7.2K RPM  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default  
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 3.2.1d released Jul-2017  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** --

### Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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<td>654.roms_s</td>
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- **SPECspeed®2017_fp_base:** 75.3
- **SPECspeed®2017_fp_peak:** 76.0
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5115, 2.40 GHz)

**SPECspeed®2017_fp_base = 75.3**

**SPECspeed®2017_fp_peak = 76.0**

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**SPECspeed®2017_fp_base = 75.3**

**SPECspeed®2017_fp_peak = 76.0**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5115, 2.40 GHz)

| SPECspeed®2017_fp_base | 75.3 |
| SPECspeed®2017_fp_peak | 76.0 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**General Notes (Continued)**

generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c454e4568ad54c135fd618b5109c0f
running on linux-uezu Mon Dec 11 16:42:42 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
  2. "physical id"s (chips)
  20 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 10
siblings : 10
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 20
- On-line CPU(s) list: 0-19
- Thread(s) per core: 1
- Core(s) per socket: 10
- Socket(s): 2

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
Stepping: 4
CPU MHz: 1148.431
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4799.99
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9
NUMA node1 CPU(s): 10-19
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hw
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnmi flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 errs invpcid rtm cqm mxp avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/procr/cpuinfo cache data
cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9
node 0 size: 192074 MB
node 0 free: 189405 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19
node 1 size: 193504 MB
node 1 free: 188263 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 394832460 kB

(Continued on next page)
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Specspeed®2017_fp_base = 75.3
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Platform Notes (Continued)

HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-uezu 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 3 15:06

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sda1      xfs   894G  150G  745G  17% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
  Memory:
     24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) |
-----------------------------------------------------------------------------
| icc (ICC) 18.0.0 20170811 |

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPEC®2017_fp_base = 75.3
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Tested by: Cisco Systems
Hardware Availability: Aug-2017

Software Availability: Sep-2017

Compiler Version Notes (Continued)

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==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
654.roms_s(base, peak)
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
628.pop2_s(base, peak)
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
Cisco Systems
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Base Portability Flags
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags
C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

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### Base Other Flags (Continued)

- Benchmarks using both Fortran and C:
  -m64 -std=c11

- Benchmarks using Fortran, C, and C++:
  -m64 -std=c11

### Peak Compiler Invocation

- **C benchmarks:**
  -icc

- **Fortran benchmarks:**
  -ifort

- Benchmarks using both Fortran and C:
  -ifort icc

- Benchmarks using Fortran, C, and C++:
  -icpc icc ifort

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

- **C benchmarks:**
  - 619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
  -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
  -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
  -DSPEC_OPENMP

  - 638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
  -DSPEC_OPENMP

  - 644.nab_s: Same as 638.imagick_s

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### Peak Optimization Flags (Continued)

Fortran benchmarks:
- `-prof-gen(pass 1)`
- `-prof-use(pass 2)`
- `-DSPEC_SUPPRESS_OPENMP`
- `-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`
- `-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp`
- `-nostandard-realloc-lhs -align array32byte`

Benchmarks using both Fortran and C:

- `621.wrf_s`: `-prof-gen(pass 1)`
- `-prof-use(pass 2)`
- `-O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`
- `-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte`

- `627.cam4_s`: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte`

- `628.pop2_s`: Same as `621.wrf_s`

Benchmarks using Fortran, C, and C++:

- `-prof-gen(pass 1)`
- `-prof-use(pass 2)`
- `-O2 -xCORE-AVX512 -qopt-prefetch`
- `-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3`
- `-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`
- `-align array32byte`

### Peak Other Flags

C benchmarks:
- `-m64 -std=c11`

Fortran benchmarks:
- `-m64`

Benchmarks using both Fortran and C:
- `-m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
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You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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