### Hardware
- **CPU Name:** Intel Xeon Platinum 8164
- **Max MHz:** 3700
- **Nominal:** 2000
- **Enabled:** 52 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 35.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 3.1.1d released Jun-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

<table>
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<td>97.1</td>
<td>1696</td>
<td>97.4</td>
</tr>
</tbody>
</table>

**Results Table**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Submit Notes**

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 222
SPECrater®2017_fp_peak = 226

General Notes (Continued)

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f
running on linux-j64x Thu Dec 14 03:12:02 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
  2 "physical id"s (chips)
  104 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 26
  siblings : 52
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28

(Continued on next page)
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

### SPEC CPU 2017 Floating Point Rate Result

![SPEC Logo](https://www.spec.org/)

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Dec-2017</th>
</tr>
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<tbody>
<tr>
<td>Hardware Availability</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

### Platform Notes (Continued)

29

From `lscpu`:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **CPU(s):** 104
- **On-line CPU(s) list:** 0-103
- **Thread(s) per core:** 2
- **Core(s) per socket:** 26
- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
- **Stepping:** 4
- **CPU MHz:** 2686.101
- **CPU max MHz:** 3700.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 3990.62
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 36608K
- **NUMA node0 CPU(s):** 0-3, 7-9, 13-15, 20-22, 52-55, 59-61, 65-67, 72-74
- **NUMA node1 CPU(s):** 4-6, 10-12, 16-19, 23-25, 56-58, 62-64, 68-71, 75-77
- **NUMA node2 CPU(s):** 26-29, 33-35, 39-41, 46-48, 78-81, 85-87, 91-93, 98-100
- **NUMA node3 CPU(s):** 30-32, 36-38, 42-45, 49-51, 82-84, 88-90, 94-97, 101-103
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt x saves xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data  
**cache size:** 36608 KB

From `numactl --hardware` WARNING: a `numactl 'node'` might or might not correspond to a physical chip.  
**available:** 4 nodes (0-3)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate\textsuperscript{\textregistered}2017\textsubscript{fp} base = 222

SPECrate\textsuperscript{\textregistered}2017\textsubscript{fp} peak = 226

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

node 0 cpus: 0 1 2 3 7 8 9 13 14 15 20 21 22 52 53 54 55 59 60 61 65 66 67 72 73 74
node 0 size: 95330 MB
node 0 free: 94913 MB
node 1 cpus: 4 5 6 7 10 11 12 16 17 18 19 23 24 25 56 57 58 62 63 64 68 69 70 71 75 76 77
node 1 size: 96760 MB
node 1 free: 96287 MB
node 2 cpus: 26 27 28 29 33 34 35 39 40 41 46 47 48 78 79 80 81 85 86 87 91 92 93 98 99
100
node 2 size: 96760 MB
node 2 free: 96442 MB
node 3 cpus: 30 31 32 36 37 38 42 43 44 45 49 50 51 82 83 84 88 89 90 94 95 96 97 101
102 103
node 3 size: 96758 MB
node 3 free: 96293 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 394864040 kB
 HugePages_Total: 0
 Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.

os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-j64x 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 222
SPECrate®2017_fp_peak = 226

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 14 02:28

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc7 xfs 416G 79G 338G 19% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |
| icc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
| icpc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak) |
| icpc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |
| icc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++, C, Fortran | 507.cactuBSSN_r(base, peak) |
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 222
SPECrate®2017_fp_peak = 226

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                 | 554.roms_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 222
SPECrate®2017_fp_peak = 226

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

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<th>SPECrate®2017_fp_base</th>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Base Other Flags

- **C benchmarks:**
  - `-m64 -std=c11`

- **C++ benchmarks:**
  - `-m64`

- **Fortran benchmarks:**
  - `-m64`

- **Benchmarks using both Fortran and C:**
  - `-m64 -std=c11`

- **Benchmarks using both C and C++:**
  - `-m64 -std=c11`

- **Benchmarks using Fortran, C, and C++:**
  - `-m64 -std=c11`

### Peak Compiler Invocation

- **C benchmarks:**
  - `icc`

- **C++ benchmarks:**
  - `icpc`

- **Fortran benchmarks:**
  - `ifort`

- **Benchmarks using both Fortran and C:**
  - `ifort icc`

- **Benchmarks using both C and C++:**
  - `icpc icc`

- **Benchmarks using Fortran, C, and C++:**
  - `icpc icc ifort`

### Peak Portability Flags

Same as Base Portability Flags
**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

**SPEC CPU 2017 Floating Point Rate Result**

<table>
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<tr>
<th>SPECrate®2017_fp_base</th>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Sep-2017

---

### Peak Optimization Flags

**C benchmarks:**

- `519.lbm_r`: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

- `538.imagick_r`: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

- `544.nab_r`: Same as `519.lbm_r`

**C++ benchmarks:**

- `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

**Fortran benchmarks:**

- `503.bwaves_r`: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`

- `549.fotonik3d_r`: Same as `503.bwaves_r`

- `554.roms_r`: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`

**Benchmarks using both Fortran and C:**

- `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`

**Benchmarks using both C and C++:**

- `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

**Benchmarks using Fortran, C, and C++:**

- `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

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### SPECrate®2017_fp_base = 222
### SPECrate®2017_fp_peak = 226

### Peak Other Flags

**C benchmarks:**
- `-m64 -std=c11`

**C++ benchmarks:**
- `-m64`

**Fortran benchmarks:**
- `-m64`

**Benchmarks using both Fortran and C:**
- `-m64 -std=c11`

**Benchmarks using both C and C++:**
- `-m64 -std=c11`

**Benchmarks using Fortran, C, and C++:**
- `-m64 -std=c11`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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