Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

| SPECrate®2017_fp_base = 76.3 | SPECrate®2017_fp_peak = 77.7 |

| CPU2017 License: 9019 | Test Date: Dec-2017 |
| Test Sponsor: Cisco Systems | Hardware Availability: Aug-2017 |
| Tested by: Cisco Systems | Software Availability: Sep-2017 |

### Hardware
- **CPU Name:** Intel Xeon Silver 4108
- **Max MHz:** 3000
- **Nominal:** 1800
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 11 MB I+D on chip per chip
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM

### Software
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 3.1.1d released Jun-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --

---

### Results
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<th>SPECrate®2017_fp_base</th>
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SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

CPU2017 License: 9019
Test Date: Dec-2017
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Hardware Availability: Aug-2017
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Results Table

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</table>

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor.

For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz) SPECrate®2017_fp_base = 76.3
SPECrate®2017_fp_peak = 77.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135f6d61bce081c0f
running on linux-3joc Fri Dec 15 11:11:33 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

(Continued on next page)
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

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</table>

### SPECrate®2017_fp_base = 76.3

### SPECrate®2017_fp_peak = 77.7

---

### Platform Notes (Continued)

```plaintext
From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
Stepping: 4
CPU MHz: 1909.505
CPU max MHz: 3000.0000
CPU min MHz: 800.0000
BogoMIPS: 3591.56
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pni pclmulqdq dtes64_64 smep cmip8 avx2 smep bmi2 3dnow epqlf aesni_intel pni pclmulqdq ds_cpl idapic�dcmp tsc_val error_monoring aes xsaveopt xsavec xsaveopt xsavec xgetbv1 cqm_100 lgro cqm_occup_llc
```

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 192091 MB
node 0 free: 191309 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Platform Notes (Continued)

node 1 size: 193518 MB  
node 1 free: 192922 MB  
node distances:  
node 0 1  
0: 10 21  
1: 21 10

From /proc/meminfo  
MemTotal: 394864760 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

```
/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2
```

From /etc/*release* /etc/*version*  
SuSE-release:  
SUSE Linux Enterprise Server 12 (x86_64)  
VERSION = 12  
PATCHLEVEL = 2

```
# This file is deprecated and will be removed in a future service pack or release.  
# Please check /etc/os-release for details about this release.
```

```
os-release:  
NAME="SLES"  
VERSION="12-SP2"  
VERSION_ID="12.2"  
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"  
ID="sles"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:  
Linux linux-3joc 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)  
x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Dec 14 03:38

**SPEC is set to:** /home/cpu2017  
**Filesystem**  
**Device**  
**Type**  
**Size**  
**Used**  
**Avail**  
**Use%**  
**Mounted on**  
```
/dev/sda3  
xfs  
516G  
114G  
403G  
22%  
/home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

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Platform Notes (Continued)

24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400
(End of data from sysinfo program)

Compiler Version Notes

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icc (ICC) 18.0.0 20170811
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Base Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icc
Benchmarks using both C and C++:
icpc icc
Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG

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**Cisco Systems**
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

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<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tbody>
<tr>
<td>76.3</td>
<td>77.7</td>
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<th>CPU2017 License</th>
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**Base Portability Flags (Continued)**

538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte

**Base Other Flags**

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPEC CPU®2017 Floating Point Rate Result
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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate®2017_fp_base = 76.3
SPECrate®2017_fp_peak = 77.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Other Flags (Continued)

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using both C and C++:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

(Continued on next page)
Peak Optimization Flags (Continued)

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch
         -ffinite-math-only -qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
         -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r

C++ benchmarks:
         -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
         -qopt-mem-layout-trans=3

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
         -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3
         -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch
         -ffinite-math-only -qopt-mem-layout-trans=3
         -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
         -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
         -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
         -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
         -qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
         -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
         -no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
         -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate®2017_fp_base = 76.3
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CPU2017 License: 9019
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Peak Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using both C and C++:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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